YOVI 2008 Core

Watch Dog Timer

(WDT)

Function Specifications

Rev 0.00

08/03/01

Rev.	Revision content	Approved	Checked	Created
0.00	New created			Duong Dang 08/03/20

Index and Table

1. Scope

This document is the Function Specification of Watch Dog Timer.

2. Features

It contains:

- Selectable from eight (WDT_0) or 16 (WDT_1) counter input clocks.
- Switchable between watchdog timer mode and interval timer mode.

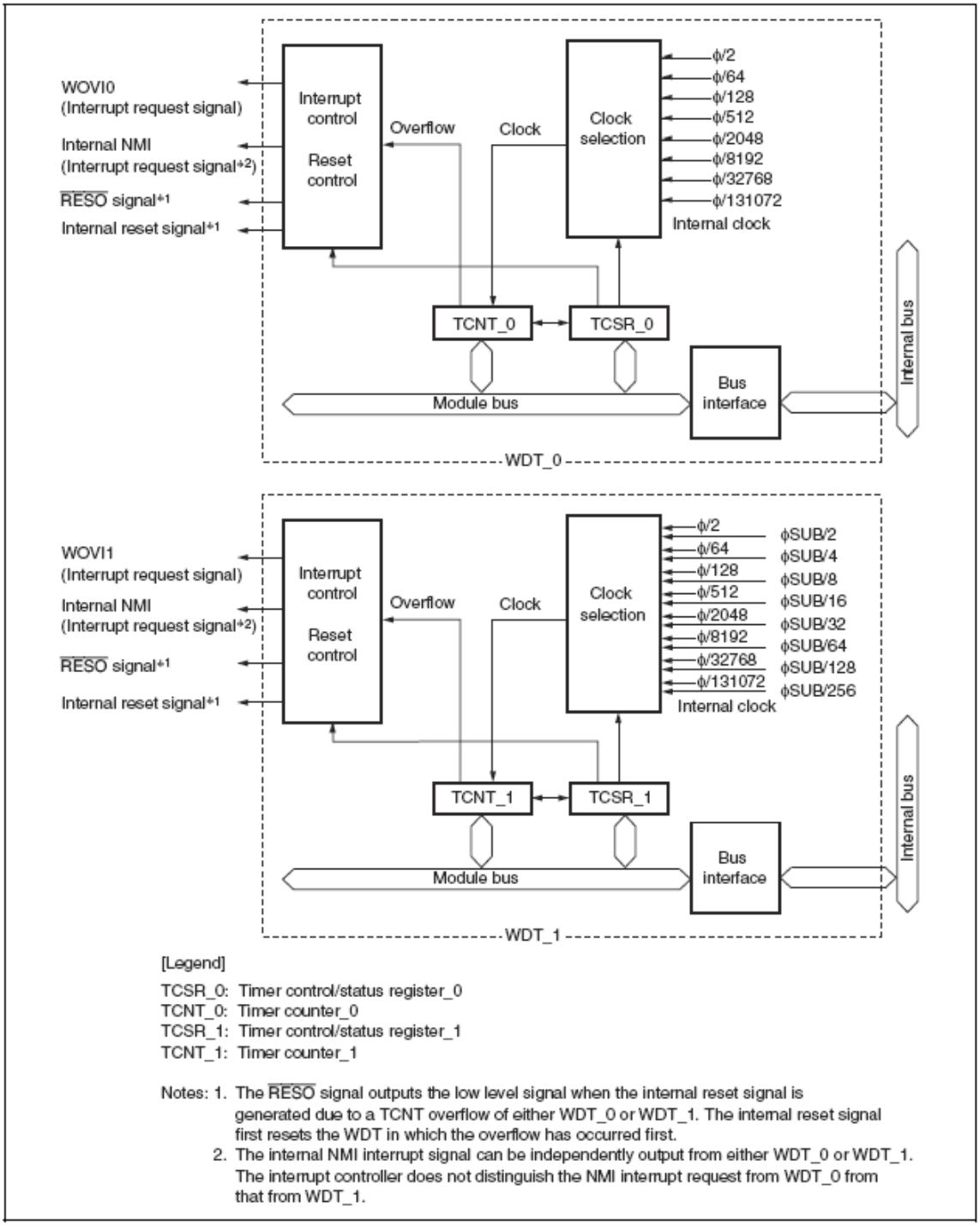
WatchdogTimer Mode:

- If the counter overflows, an internal reset or an internal NMI interrupt is generated.
- When the LSI is selected to be internally reset at counter overflow, a low level signal is output from the RESO pin if the counter overflows.

Internal Timer Mode:

- If the counter overflows, an internal timer group (WOVI) is generated.

3. Block Diagram



[Legend]

TCSR_0: Timer control/status register_0
TCNT_0: Timer counter_0
TCSR_1: Timer control/status register_1
TCNT_1: Timer counter_1

Notes: 1. The RESO signal outputs the low level signal when the internal reset signal is generated due to a TCNT overflow of either WDT_0 or WDT_1. The internal reset signal first resets the WDT in which the overflow has occurred first.
2. The internal NMI interrupt signal can be independently output from either WDT_0 or WDT_1. The interrupt controller does not distinguish the NMI interrupt request from WDT_0 from that from WDT_1.

Figure 3.1: FRT block diagram

4. Port Description

Table below shows the FRT port descriptions

Name	I/O	Function
$\overline{RESO}$	Output	Outputs the counter overflow signal in watchdog timer mode
EXCL	Input	Inputs the clock pulse to the WDT_1 prescaler counter

5. Register Description

This WDT has the following registers:

- Timer Counter (TCNT)
- Timer Control Status Register (TCSR)

5.1 Timer Counter (TCNT)

Bit	7	6	5	4	3	2	1	0
	TCNT7	**TCNT6**	**TCNT5**	**TCNT4**	**TCNT3**	**TCNT2**	**TCNT1**	**TCNT0**
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.2 Timer Control Status Register (TCSR)

TCSR selects the clock source to be input to TCNT, and the timer mode.

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	**TME**	**—**	RST/$\overline{NMI}$	**CKS2**	**CKS1**	**CKS0**
Initial value								
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- TCSR_0

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting conditions] • When TCNT overflows (changes from H'FF to H'00) • When internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] • When TCSR is read when OVF = 1, then 0 is written to OVF • When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode

5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
4	—	0	R/W	Reserved The initial value should not be changed.
3	RST/$\overline{\text{NMI}}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested
2 to 0	CKS2 to CKS0	All 0	R/W	Clock Select 2 to 0 Select the clock source to be input to TCNT. The overflow frequency for ϕ = 33 MHz is enclosed in parentheses. 000: ϕ/2 (frequency: 15.5 µs) 001: ϕ/64 (frequency: 496.5 µs) 010: ϕ/128 (frequency: 993.0 µs) 011: ϕ/512 (frequency: 4.0 ms) 100: ϕ/2048 (frequency: 15.9 ms) 101: ϕ/8192 (frequency: 63.6 ms) 110: ϕ/32768 (frequency: 254.2 ms) 111: ϕ/131072 (frequency: 1.02 s)

Note: * Only 0 can be written, to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting conditions] • When TCNT overflows (changes from H'FF to H'00) • When internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] • When TCSR is read when OVF = 1*[2], then 0 is written to OVF • When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
4	PSS	0	R/W	Prescaler Select Selects the clock source to be input to TCNT. 0: Counts the divided cycle of ϕ–based prescaler (PSM) 1: Counts the divided cycle of ϕSUB–based prescaler (PSS)
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested

2 to 0	CKS2 to CKS0	All 0	R/W	Clock Select 2 to 0 Select the clock source to be input to TCNT. The overflow cycle for ϕ = 33 MHz and ϕSUB = 32.768 kHz is enclosed in parentheses. When PSS = 0: 000: ϕ/2 (frequency: 15.5 µs) 001: ϕ/64 (frequency: 496.5 µs) 010: ϕ/128 (frequency: 993.0 µs) 011: ϕ/512 (frequency: 4.0 ms) 100: ϕ/2048 (frequency: 15.9 ms) 101: ϕ/8192 (frequency: 63.6 ms) 110: ϕ/32768 (frequency: 254.2 ms) 111: ϕ/131072 (frequency: 1.02 s) When PSS = 1: 000: ϕSUB/2 (cycle: 15.6 ms) 001: ϕSUB/4 (cycle: 31.3 ms) 010: ϕSUB/8 (cycle: 62.5 ms) 011: ϕSUB/16 (cycle: 125 ms) 100: ϕSUB/32 (cycle: 250 ms) 101: ϕSUB/64 (cycle: 500 ms) 110: ϕSUB/128 (cycle: 1 s) 111: ϕSUB/256 (cycle: 2 s)

Notes: 1. Only 0 can be written, to clear the flag.
2. When OVF is polled with the interval timer interrupt disabled, OVF = 1 must be read at least twice.

6. Operation

6.1 Watchdog Timer Mode

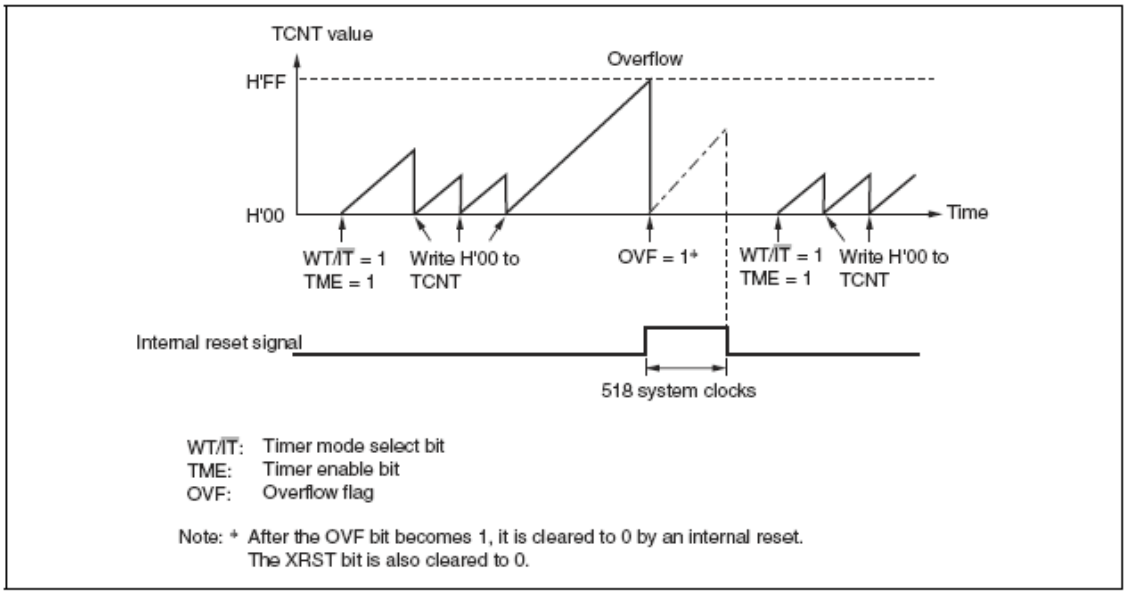


Figure 6.1: Watchdog Timer Mode ($\overline{RST}/\overline{NMI} = 1$) Operation

6.2 Interval Timer Mode

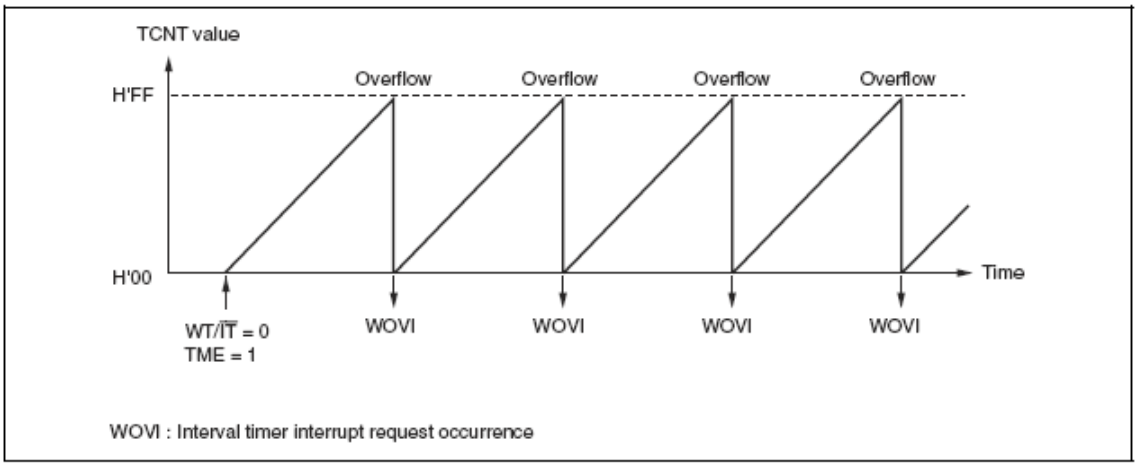


Figure 6.2: Interval Timer Mode Operation

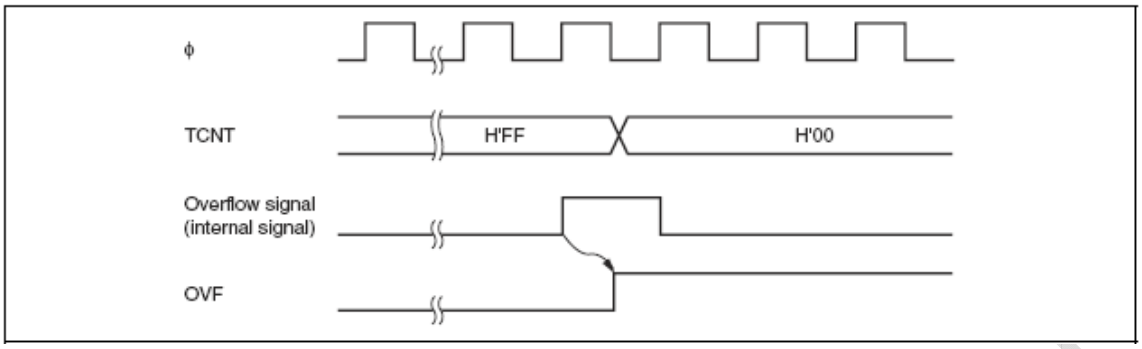


Figure 6.3: OVF Flag Set Timing

6.3 RESO Signal Output Timing

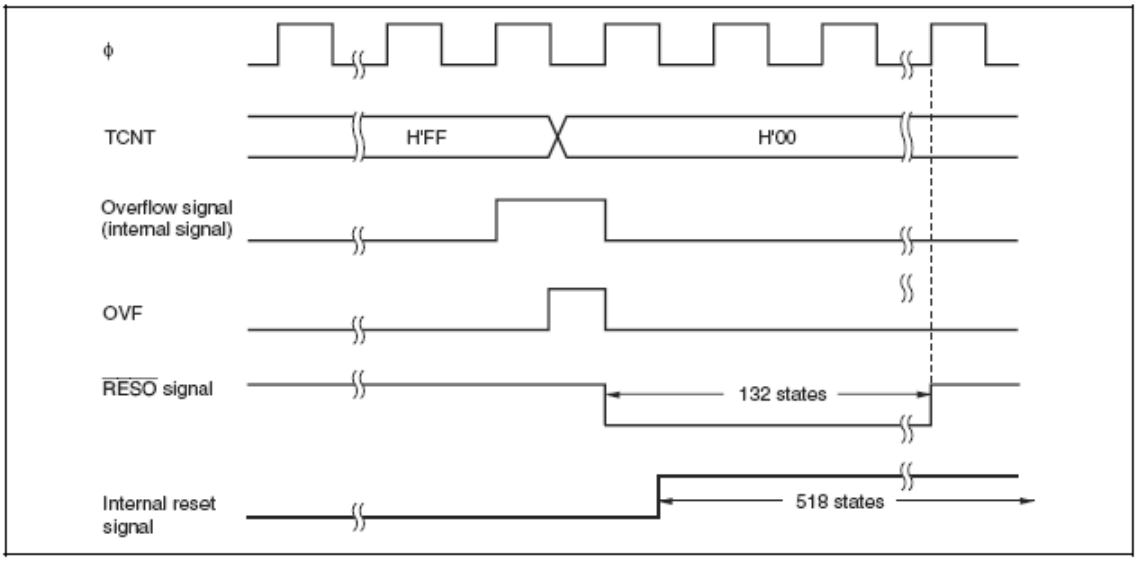


Figure 6.4: Output of RESO signal

-End-