YOVI 2008 Core

16-Bit Free-Running Timer

(FRT)

Function Specifications

Rev 0.00

08/07/10

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0.00	New created			Duong Dang 08/07/10

Index and Table

1. Scope

This document is the Function Specification of 16-Bit Free Running Timer.

2. Features

FRT is operates on the basic of the 16-Bit Free-running counter (FRC).

It contains:

- Selection of four clock sources
- Two independent comparators
- Four independent capture input channels
- Counter clearing
- Seven independent interrupts
- Special functions provided by automatic addition function

3. Block Diagram

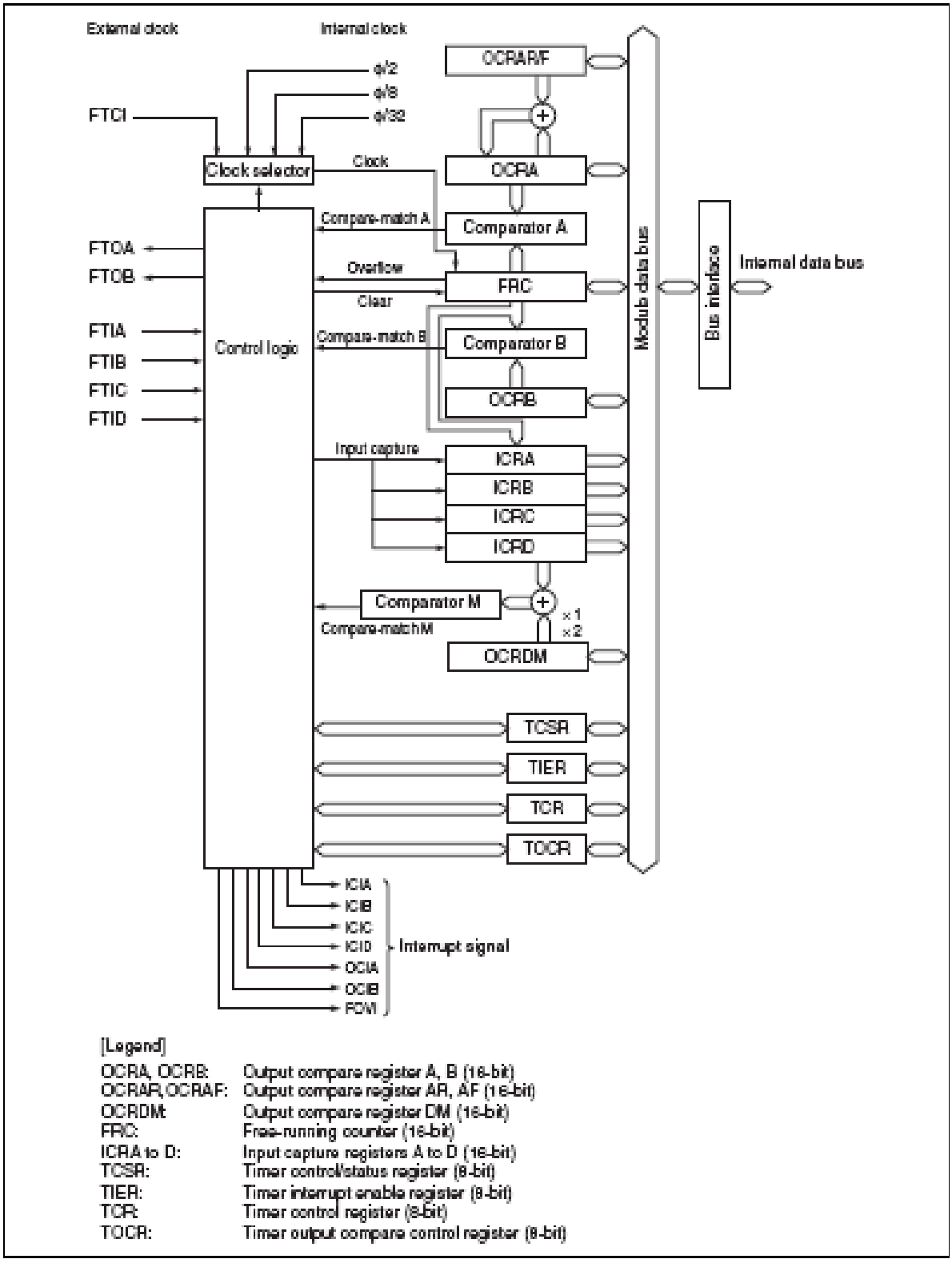

Figure 3.1: FRT block diagram

4. Port Descriptions

Table below shows the FRT port descriptions

Name	I/O	Function
FTIC	Input	FRC counter clock input
FTOA	Output	Output compare A output
FTOB	Output	Output compare B output
FTIA	Input	Input capture A input
FTIB	Input	Input capture B input
FTIC	Input	Input capture C input
FTID	Input	Input capture D input

Table 4.1: Port Description

5. Register Descriptions

This FRC has the following registers:

- Free-running counter (FRC)
- Output compare register A (OCRA)
- Output compare register B (OCRB)
- Input capture register A (ICRA)
- Input capture register A (ICRB)
- Input capture register A (ICRC)
- Input capture register A (ICRD)
- Output compare register AR (OCRAR)
- Output compare register AF (OCRAF)
- Output compare register DM (OCRDM)

- Timer interrupt enable register (TIER)
- Timer control/status register (TCSR)
- Timer control register (TCR)
- Timer output compare control register (TOCR)

5.1 Free-running counter (FRC)

FRC:

- Is a 16 bit readable/writable up-counter that increments on an internal pulse generated from a clock source.
- Selected the clock source by the clock select 1 and 0 bits (CKS1 and CKS0) of the timer control register (TCR).
- Is initialized to H'0000 and can be cleared by compare-match A.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.2 Output Compare Register A and B (OCRA and OCRB)

OCRA and OCRB:

- They are 16-bit readable/writable register whose content are compared with the value of FRC.
- When a match is detected, the corresponding output compare flag (OCFA or OCFB) is set in the timer control/status register (TCSR).
- If the output enable bit (OEA or OEB) in the timer control register (TCR) is set to "1", when the output compare register and FRC values match, the logic level selected by the output level bit (OLVLA or OLVLB) in the timer control status register (TCSR) is output at the output compare pin (FTOA or FTOB).

- The FTOA and FTOB output are “0” before the first compare-match.
- OCRA and OCRB are initialized H’FFFF.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.3 Input Capture Registers A to D (ICRA to ICRD)

Each input capture register:

- 16-bit read only register.
- When the rising or falling edge of the signal at the input capture input pin is detected, the current value of the FRC is copied to the ICR.
- At the same time, the input capture flag (ICF) in the timer control status register (TCSR) is set to “1”.
- The input capture edge is selected by the input edge select bit (IEDG) in the TCSR.
- The pulse width of the input capture signal should be at least 1.5 system to ensure the input capture.
- It is initialized H’0000.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

5.4 Output Compare Register AR and AF (OCRAR and OCRAF)

OCRAR and OCRAF:

- 16-bit readable/writable register.
- The contents of OCRAR and OCRAF are added alternately to OCRA when the OCRAMS bit in TOCR is set to 1.
- The write operation is performed on the occurrence of compare-match A.
- IOCRAF is added in the first compare-match A after setting the OCRAMS bit to 1.
- The value of OLVLA bit in TOCR is ignored.
- 1 is output on a compare-match A following addition of OCRAF, and 0 is output on a compare-match A following addition of OCRAR.
- Both of registers are initialized to H'FFFF.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.5 Output Compare Register DM (OCRDM)

OCRDM:

- A 16-bit readable/writable register, upper eight bits are fixed at H'00.
- Operation of ICRD is changed to include the use of OCRDM
  - ICRDMS bit in TOCR is set to 1.
  - The contents of OCRDM are other than H'00.
- The start of mask interval is the point at which input capture D occurs.

- The end of mask interval is the point at which the values match is taken.
- During mask interval, new input capture D events are disabled.
- A mask interval is not generated when the contents of OCRDM are H'00 while the ICRDMS bit is set to 1.
- It is initialized to H'0000.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.6 Timer Interrupt Enable Register (TIER)

TIER:

- Is an 8-bit register readable/writable register.
- Enable and disable interrupt request.
- Is initialized to H'00.

Bit	7	6	5	4	3	2	1	0
	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
7	ICIAE	0	R/W	Input Capture Interrupt A Enable Selects whether to enable input capture interrupt A request (ICIA) when input capture flag A (ICFA) in TCSR is set to 1. 0: ICIA requested by ICFA is disabled 1: ICIA requested by ICFA is enabled
6	ICIBE	0	R/W	Input Capture Interrupt B Enable Selects whether to enable input capture interrupt B request (ICIB) when input capture flag B (ICFB) in TCSR is set to 1. 0: ICIB requested by ICFB is disabled 1: ICIB requested by ICFB is enabled
5	ICICE	0	R/W	Input Capture Interrupt C Enable Selects whether to enable input capture interrupt C request (ICIC) when input capture flag C (ICFC) in TCSR is set to 1. 0: ICIC requested by ICFC is disabled 1: ICIC requested by ICFC is enabled
4	ICIDE	0	R/W	Input Capture Interrupt D Enable Selects whether to enable input capture interrupt D request (ICID) when input capture flag D (ICFD) in TCSR is set to 1. 0: ICID requested by ICFD is disabled 1: ICID requested by ICFD is enabled
3	OCIAE	0	R/W	Output Compare Interrupt A Enable Selects whether to enable output compare interrupt A request (OCIA) when output compare flag A (OCFA) in TCSR is set to 1. 0: OCIA requested by OCFA is disabled 1: OCIA requested by OCFA is enabled

2	OCIBE	0	R/W	Output Compare Interrupt B Enable Selects whether to enable output compare interrupt B request (OCIB) when output compare flag B (OCFB) in TCSR is set to 1. 0: OCIB requested by OCFB is disabled 1: OCIB requested by OCFB is enabled
1	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether to enable a free-running timer overflow request interrupt (FOVI) when the timer overflow flag (OVF) in TCSR is set to 1. 0: FOVI requested by OVF is disabled 1: FOVI requested by OVF is enabled
0	—	0	R	Reserved This bit is always read as 1 and cannot be modified.

5.7 Timer Control/Status Register (TCSR)

TCSR:

- A readable/writable register.
- Used for counter clear selection and control of interrupt request signal.
- Is initialized to H'00.

Bit	7	6	5	4	3	2	1	0
	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ICFA	0	R/(W)*	Input Capture Flag A This status flag indicates that the FRC value has been transferred to ICRA by means of an input capture signal. When BUFEA = 1, ICFA indicates that the old ICRA value has been moved into ICRC and the new FRC value has been transferred to ICRA. [Setting condition] When an input capture signal causes the FRC value to be transferred to ICRA [Clearing condition] Read ICFA when ICFA = 1, then write 0 to ICFA
6	ICFB	0	R/(W)*	Input Capture Flag B This status flag indicates that the FRC value has been transferred to ICRB by means of an input capture signal. When BUFEB = 1, ICFB indicates that the old ICRB value has been moved into ICRD and the new FRC value has been transferred to ICRB. [Setting condition] When an input capture signal causes the FRC value to be transferred to ICRB [Clearing condition] Read ICFB when ICFB = 1, then write 0 to ICFB
5	ICFC	0	R/(W)*	Input Capture Flag C This status flag indicates that the FRC value has been transferred to ICRC by means of an input capture signal. When BUFEA = 1, on occurrence of an input capture signal specified by the IEDGC bit at the FTIC input pin, ICFC is set but data is not transferred to ICRC. In buffer operation, ICFC can be used as an external interrupt signal by setting the ICICE bit to 1. [Setting condition] When an input capture signal is received [Clearing condition] Read ICFC when ICFC = 1, then write 0 to ICFC
4	ICFD	0	R/(W)*	Input Capture Flag D This status flag indicates that the FRC value has been transferred to ICRD by means of an input capture signal. When BUFEB = 1, on occurrence of an input capture signal specified by the IEDGD bit at the FTID input pin, ICFD is set but data is not transferred to ICRD. In buffer operation, ICFD can be used as an external interrupt signal by setting the ICIDE bit to 1. [Setting condition] When an input capture signal is received [Clearing condition] Read ICFD when ICFD = 1, then write 0 to ICFD

3	OCFA	0	R/(W)*	Output Compare Flag A This status flag indicates that the FRC value matches the OCRA value. [Setting condition] When FRC = OCRA [Clearing condition] Read OCFA when OCFA = 1, then write 0 to OCFA
2	OCFB	0	R/(W)*	Output Compare Flag B This status flag indicates that the FRC value matches the OCRB value. [Setting condition] When FRC = OCRB [Clearing condition] Read OCFB when OCFB = 1, then write 0 to OCFB
1	OVF	0	R/(W)*	Overflow Flag This status flag indicates that the FRC has overflowed. [Setting condition] When FRC overflows (changes from H'FFFF to H'0000) [Clearing condition] Read OVF when OVF = 1, then write 0 to OVF
0	CCLRA	0	R/W	Counter Clear A This bit selects whether the FRC is to be cleared at compare-match A (when the FRC and OCRA values match). 0: FRC clearing is disabled 1: FRC is cleared at compare-match A

Note: * Only 0 can be written to clear the flag.

5.8 Timer Control Register (TCR)

TCR:

- Is an 8-bit register readable/writable register.
- Selects the rising or falling edge of the input capture signals.
- Enables the input capture buffer mode.
- Selects the FRC clock source.
- Is initialized H’00.

Bit	7	6	5	4	3	2	1	0
	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0

Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	IEDGA	0	R/W	Input Edge Select A Selects the rising or falling edge of the input capture A signal (FTIA). 0: Capture on the falling edge of FTIA 1: Capture on the rising edge of FTIA
6	IEDGB	0	R/W	Input Edge Select B Selects the rising or falling edge of the input capture B signal (FTIB). 0: Capture on the falling edge of FTIB 1: Capture on the rising edge of FTIB
5	IEDGC	0	R/W	Input Edge Select C Selects the rising or falling edge of the input capture C signal (FTIC). 0: Capture on the falling edge of FTIC 1: Capture on the rising edge of FTIC
4	IEDGD	0	R/W	Input Edge Select D Selects the rising or falling edge of the input capture D signal (FTID). 0: Capture on the falling edge of FTID 1: Capture on the rising edge of FTID
3	BUFEA	0	R/W	Buffer Enable A Selects whether ICRC is to be used as a buffer register for ICRA. 0: ICRC is not used as a buffer register for ICRA 1: ICRC is used as a buffer register for ICRA
2	BUFEB	0	R/W	Buffer Enable B Selects whether ICRD is to be used as a buffer register for ICRB. 0: ICRD is not used as a buffer register for ICRB 1: ICRD is used as a buffer register for ICRB
1	CKS1	0	R/W	Clock Select 1 and 0
0	CKS0	0	R/W	Select clock source for FRC. 00: φ/2 internal clock source 01: φ/8 internal clock source 10: φ/32 internal clock source 11: External clock source (counting at FTCI rising edge)

5.9 Timer Output Compare Control Register (TOCR)

TOCR:

- Is an 8-bit readable/writable register.
- Enables output from the output compare pins.
- Selects the output levels.
- Switches access between output compare register A and B.
- Controls the ICRD and OCRA operating modes.
- Switches access to input capture registers A, B and C.
- Is initialized to H'00.

Bit	7	6	5	4	3	2	1	0
	ICRDMS	ICRAMS	ICRS	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ICRDMS	0	R/W	Input Capture D Mode Select Specifies whether ICRD is used in the normal operating mode or in the operating mode using OCRDM. 0: The normal operating mode is specified for ICRD 1: The operating mode using OCRDM is specified for ICRD
6	OCRAMS	0	R/W	Output Compare A Mode Select Specifies whether OCRA is used in the normal operating mode or in the operating mode using OCRAR and OCRAF. 0: The normal operating mode is specified for OCRA 1: The operating mode using OCRAR and OCRAF is specified for OCRA
5	ICRS	0	R/W	Input Capture Register Select The same addresses are shared by ICRA and OCRAR, by ICRB and OCRAF, and by ICRC and OCRDM. The ICRS bit determines which registers are selected when the shared addresses are read from or written to. The operation of ICRA, ICRB, and ICRC is not affected. 0: ICRA, ICRB, and ICRC are selected 1: OCRAR, OCRAF, and OCRDM are selected

4	OCRS	0	R/W	Output Compare Register Select OCRA and OCRB share the same address. When this address is accessed, the OCRS bit selects which register is accessed. The operation of OCRA or OCRB is not affected. 0: OCRA is selected 1: OCRB is selected
3	OEA	0	R/W	Output Enable A Enables or disables output of the output compare A output pin (FTOA). 0: Output compare A output is disabled 1: Output compare A output is enabled
2	OEB	0	R/W	Output Enable B Enables or disables output of the output compare B output pin (FTOB). 0: Output compare B output is disabled 1: Output compare B output is enabled
1	OLVLA	0	R/W	Output Level A Selects the level to be output at the output compare A output pin (FTOA) in response to compare-match A (signal indicating a match between the FRC and OCRA values). When the OCRAMS bit is 1, this bit is ignored. 0: 0 is output at compare-match A 1: 1 is output at compare-match A
0	OLVLB	0	R/W	Output Level B Selects the level to be output at the output compare B output pin (FTOB) in response to compare-match B (signal indicating a match between the FRC and OCRB values). 0: 0 is output at compare-match B 1: 1 is output at compare-match B

6. Operation

6.1 FRC Increment Timing

FRC Increment Timing:

- Increments on a pulse generated once for each period of the selected (internal or external) clock source.
- The pulse width of the external clock signal must be at least 1.5 ø clock periods. The counter will not increment correctly if the pulse width is shorter than 1.5 ø clock periods.

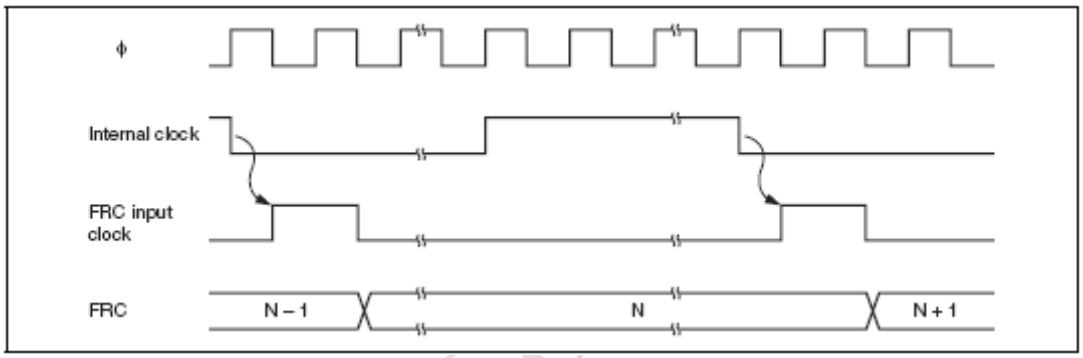

Figure 6.1: Increment Timing with the Internal Clock Source

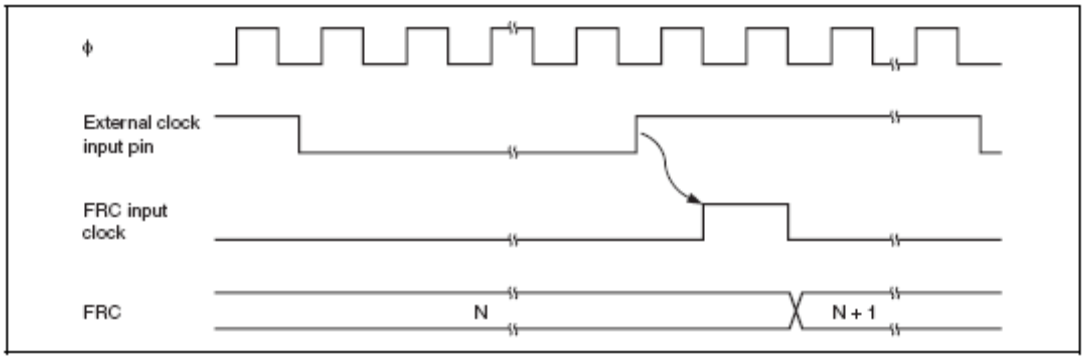

Figure 6.2: Increment Timing with the External Clock Source

6.2 Output Compare Output Timing

Setting of Output Compare Flags A and B: A compare-match signal occurs:

- At the last state when FRC and OCR values match (at the timing when the FRC updates the counter values).
- The level selected by OLVL bit in TOCR is output at the output compare pin (FTOA or FTOB).

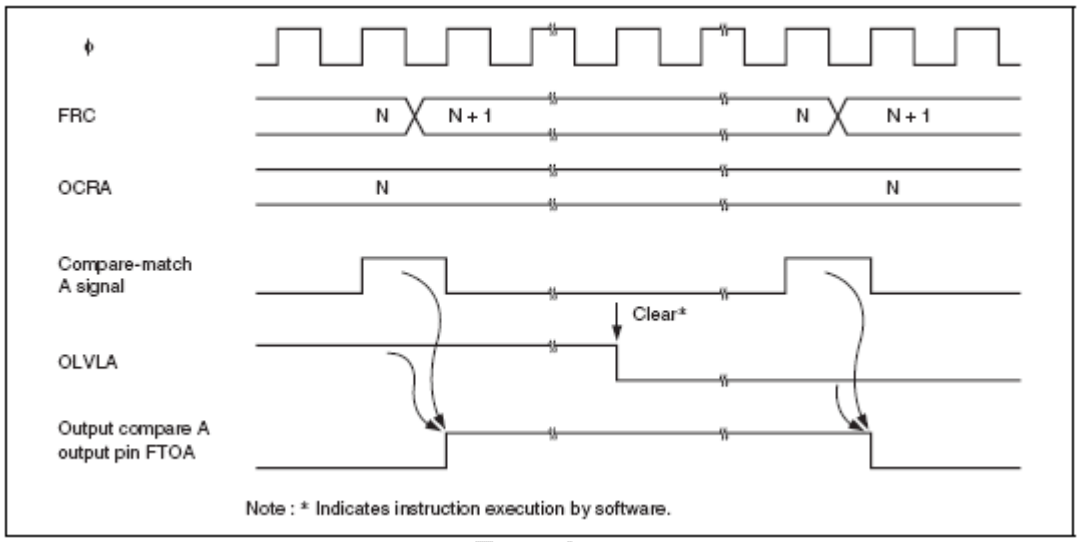

Figure 6.3: Timing of Output Compare A Output

6.3 FRC Clear Timing

FRC can be cleared when compare-match A occurs

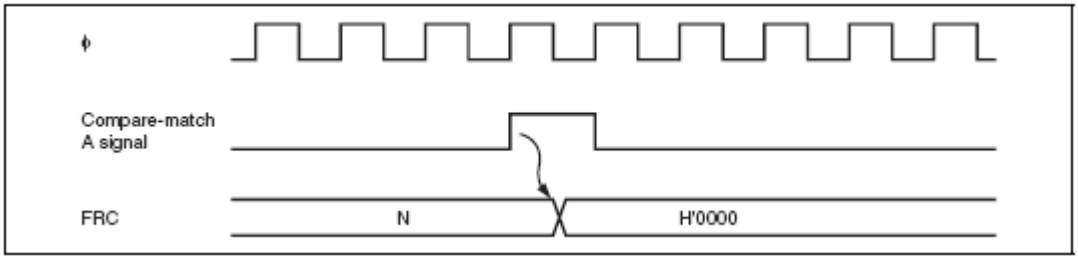

Figure 6.4: Clearing of FRC by Compare-Match A Signal

6.4 Input Capture Input Timing

Input Capture Timing:

- An internal input capture signal is generated from the rising or falling edge of the input capture input timing by the IEDGA to IEDGD bits In TCR

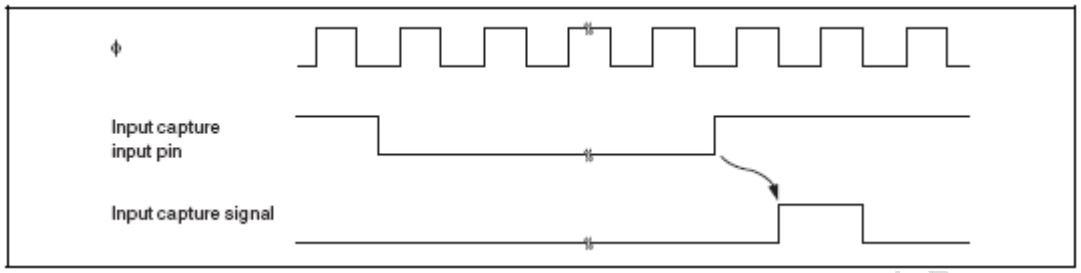

Figure 6.5: Input Capture Input Signal Timing (Usual Case)

But if ICRA and ICRD are read when the corresponding input capture signal arrives, the internal input capture signal is delayed by one system clock.

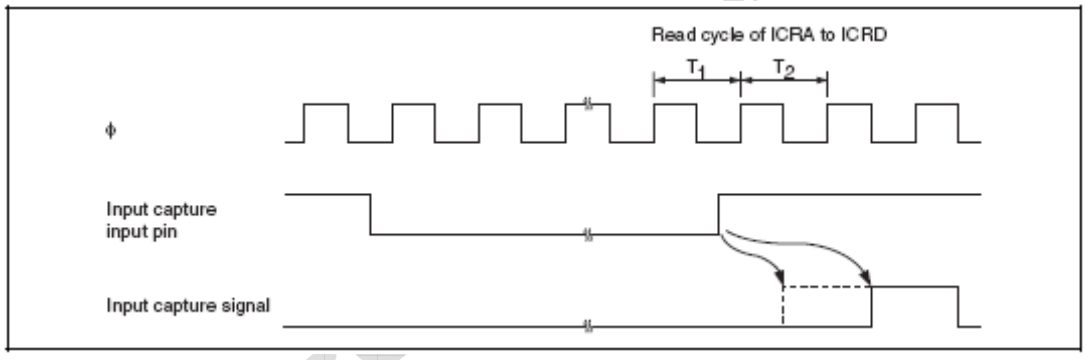

Figure 6.6: Input Capture Input Signal Timing

(When ICRA to ICRD is read)

6.5 Buffered Input Capture Input Timing

ICRC and ICRD can operate as buffers for ICRA and ICRB respectively.

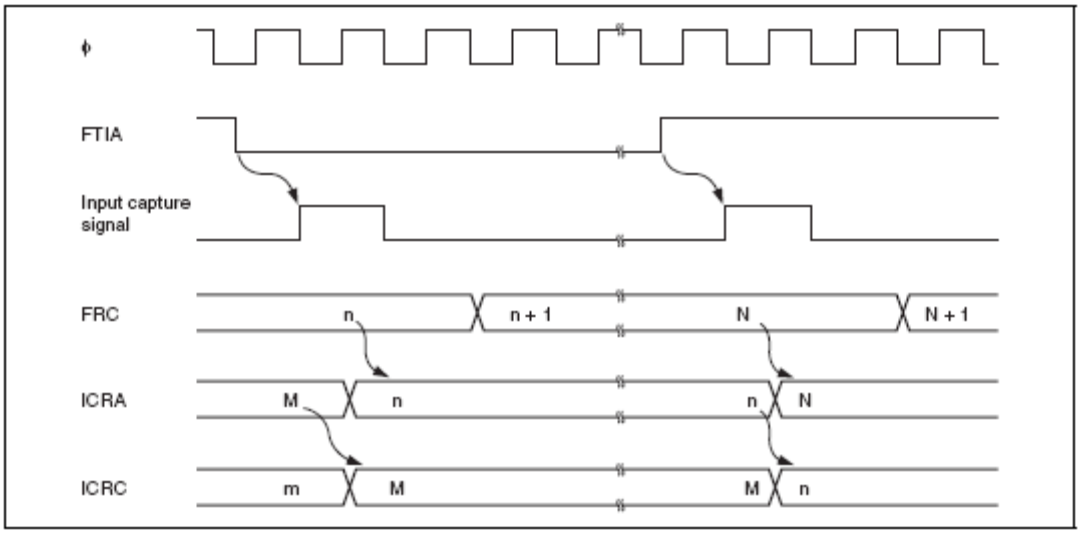

Figure 6.7: Buffered Input Capture Timing

In the figure above, ICRC is used to buffer ICRA, when the edge transition selected by the IEDGC bit occurs on the FTIC input capture line:

- ICFC will be set.
- If the ICICE bit is set at this time, an interrupt will be request.
- FRC value will not be transferred to ICRC.

But in buffered input capture, if either set of two registers to which data will be transferred (ICRA and ICRC, or ICRB and ICRD) is being read when the input capture input signal arrives, input capture is delayed by one system clock.

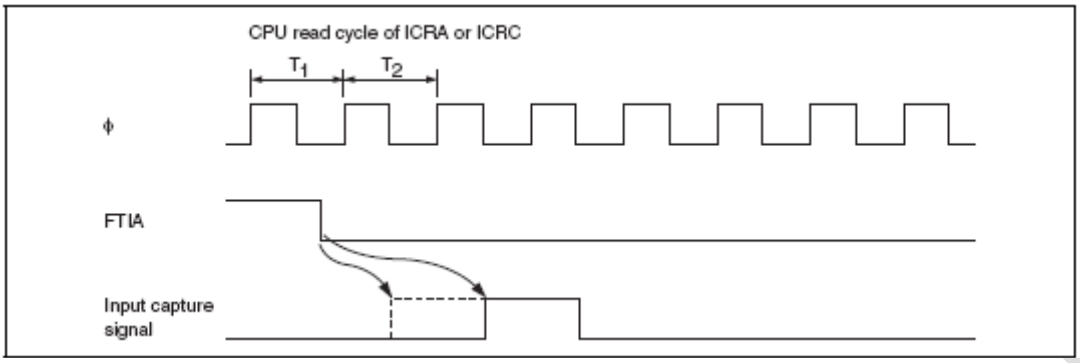

Figure 6.8: Buffered Input Capture Timing (BUFEA = 1)

6.6 Timing of Input Capture Flag (ICF) Setting

The input capture flag (ICFA to ICFD) is set to "1" by the internal input capture signal.

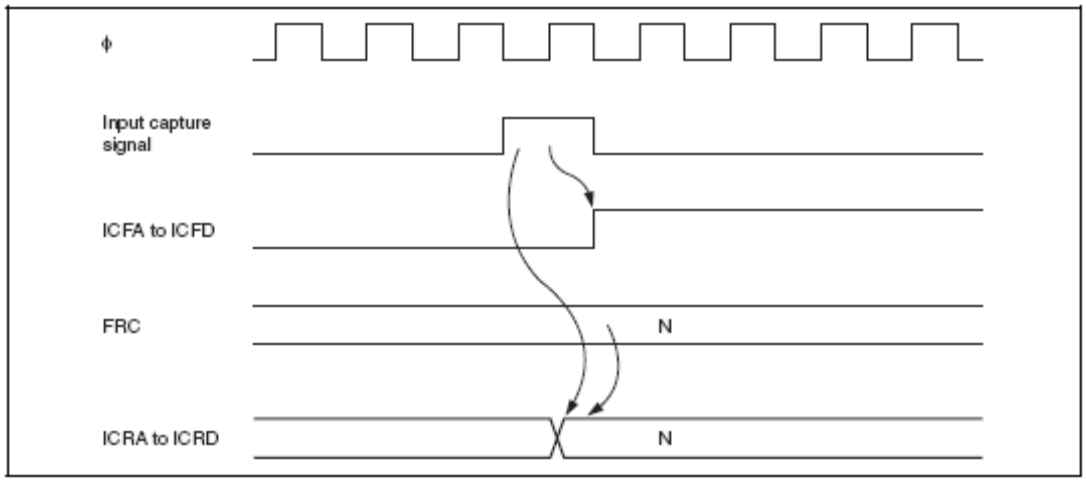

Figure 6.9: Timing of Input Capture Flag (ICFA to ICFD) Setting

6.7 Timing of Output Compare Flag (OCF) Setting

The output compare flag, OCFA or OCFB is set to 1 by compare-match signal generated when the FRC value matches the OCRA or OCRB value.

This compare-match signal is generated at the last state in which the two values match, just before FRC increments to new value.

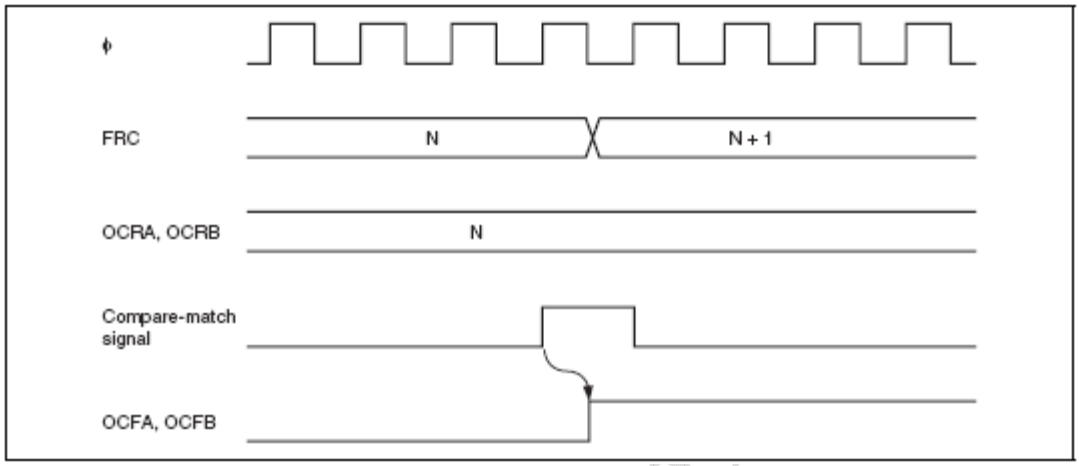

Figure 6.10: Timing of Output Compare Flag (OCFA or OCFB) Setting

6.8 Timing of FRC Overflow Flag (OVF) Setting

The FRC overflow flag (OVF) is set to 1 when FRC overflows (changes from H'FFFF to H'0000).

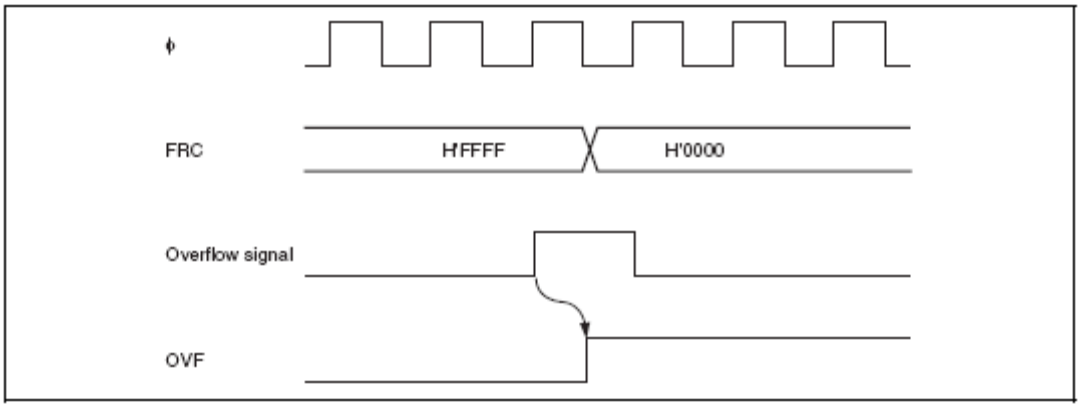

Figure 6.11: Timing of Overflow Flag (OVF) Setting

6.9 Automatic Addition Timing

OCRAMS bit in TOCR is set to 1, the contents of OCRAR and OCRAF are added to OCRA alternately.

An OCRA compare-match occurs a write to OCRA is performed.

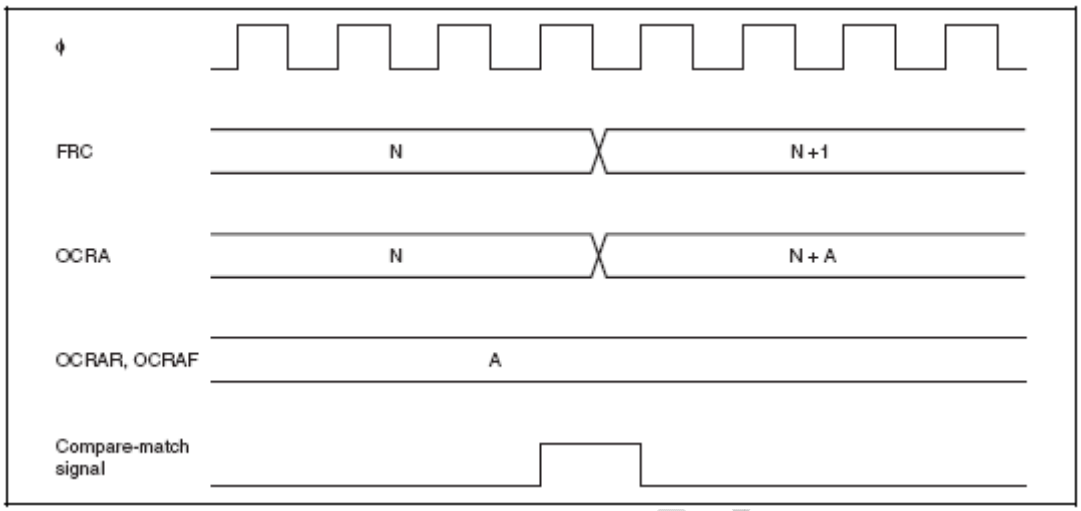

Figure 6.12: OCRA Automatic Addition Timing

6.10 Mask Signal Generation Timing

A signal that masks the ICRD input capture signal is generated:

- ICRDMS bit in TOCR is set to 1.
- The contents of OCRDM are other than H'0000.

The mask:

- Is set by the input capture signal.
- Is cleared by the sum of the ICRD contents and twice the OCRDM contents and an FRC compare-match.

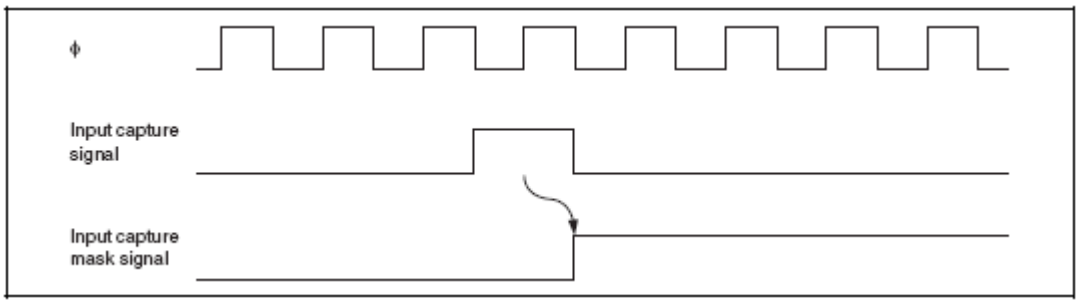

Figure 6.13: Timing of Input Capture Mask Signal Generation Timing

-End-