14-Bit PWM Timer (PWM)

This LSI has an on-chip 14-bit pulse-width modulator (PWM) timer with four output channels. It can be connected to an external low-pass filter to operate as a 14-bit D/A converter.

10.1 Features

Division of pulse into multiple base cycles to reduce ripple
Eight resolution settings
The resolution can be set to 1, 2, 64, 128, 256, 1024, 4096, or 16384 system clock cycles.
Two base cycle settings
The base cycle can be set equal to T · 64 or T · 256, where T is the resolution.
Sixteen operation clocks (by combination of eight resolution settings and two base cycle settings)

Figure 10.1 shows a block diagram of the PWM (D/A) module.

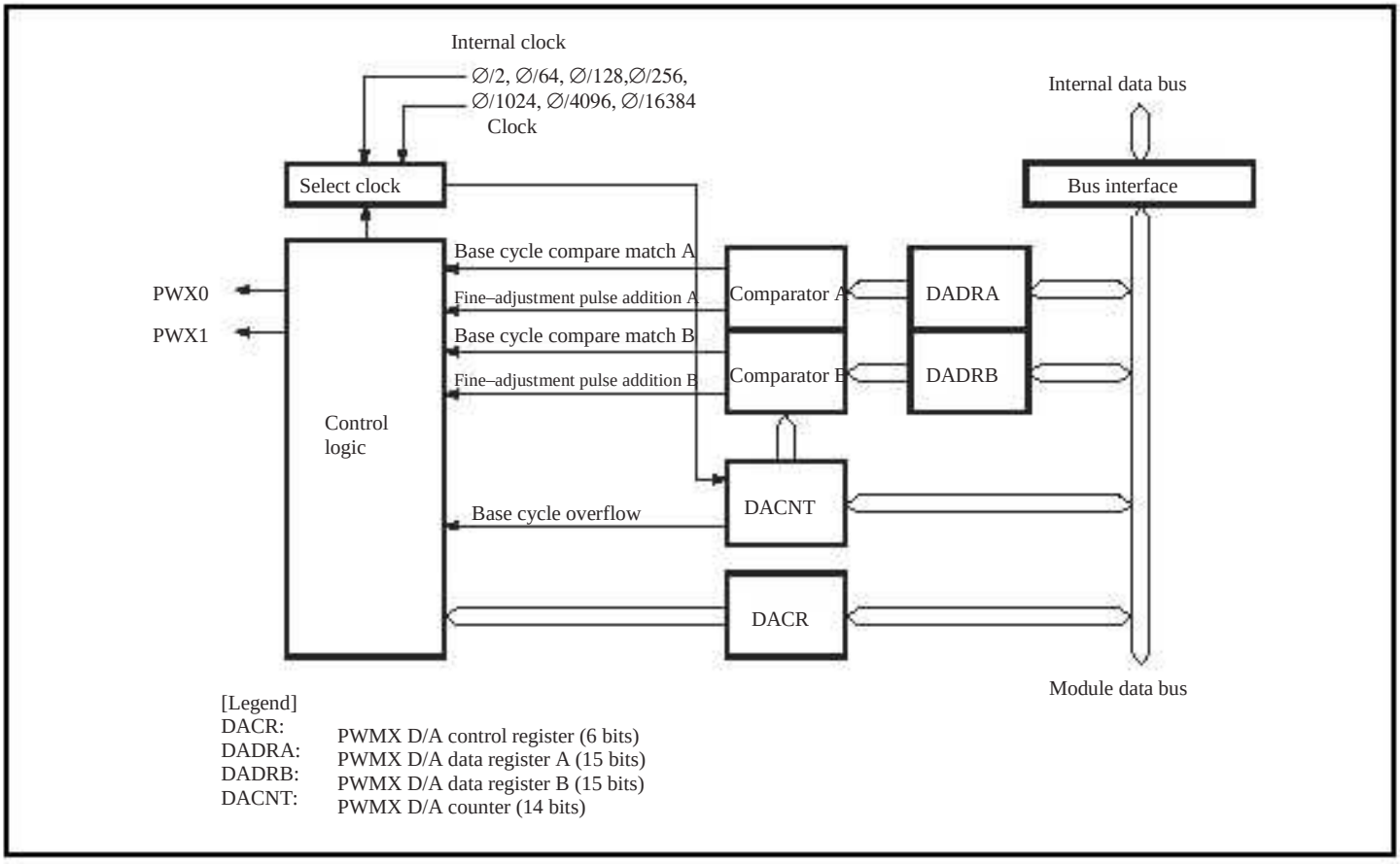


Figure 10.1 PWMX (D/A) Block Diagram

10.2 Input/Output Pins

Table 10.1 lists the PWMX (D/A) module input and output pins.

Table 10.1 Pin Configuration

Name	Abbreviation	I/O	Function
PWMX output pin 0	PWX0	Output	PWM timer pulse output of PWMX_0 channel A
PWMX output pin 1	PWX1	Output	PWM timer pulse output of PWMX_0 channel B
PWMX output pin 2	PWX2	Output	PWM timer pulse output of PWMX_1 channel A
PWMX output pin 3	PWX3	Output	PWM timer pulse output of PWMX_1 channel B

10.3 Register Descriptions

The PWMX (D/A) module has the following registers. The PWMX (D/A) registers are assigned to the same addresses with other registers. The registers are selected by the IICE bit in the serial timer control register (STCR). For details on the module stop control register, see section 23.1.3, Module Stop Control Register H, L, and A (MSTPCRH, MSTPCRL, MSTPCRA).

PWMX (D/A) counter (DACNT)
PWMX (D/A) data register A (DADRA)
PWMX (D/A) data register B (DADRB)
PWMX (D/A) control register (DACR)
Peripheral clock select register (PCSR)

Note: The same addresses are shared by DADRA and DACR, and by DADRB and DACNT. Switching is performed by the REGS bit in DACNT or DADRB.

10.3.1 PWMX (D/A) Counter (DACNT)

DACNT is a 14-bit readable/writable up-counter. The input clock is selected by the clock select bit (CKS) in DACR. DACNT functions as the time base for both PWMX (D/A) channels. When a channel operates with 14-bit precision, it uses all DACNT bits. When a channel operates with 12-bit precision, it uses the lower 12 bits and ignores the upper two bits. DACNT cannot be accessed in 8-bit units. DACNT should always be accessed in 16-bit units. For details, see section 10.4, Bus Master Interface.

DACNT

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	UC7 to UC0	All 0	R/W	Lower Up-Counter
7 to 2	UC8 to UC13	All 0	R/W	Upper Up-Counter
1		1	R	Reserved This bit is always read as 1 and cannot be modified.
0	REGS	1	R/W	Register Select DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. When changing the register to be accessed, set this bit in advance. 0: DADRA and DADRB can be accessed 1: DACR and DACNT can be accessed

10.3.2 PWMX (D/A) Data Registers A and B (DADRA and DADRB)

DADRA corresponds to PWMX (D/A) channel A, and DADRB to PWMX (D/A) channel B. The DADR registers cannot be accessed in 8-bit units. The DADR registers should always be accessed in 16-bit units. For details, see section 10.4, Bus Master Interface.

DADRA

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	DA13 to DA0	All 1	R/W	D/A Data 13 to 0 These bits set a digital value to be converted to an analog value. In each base cycle, the DACNT value is continually compared with the DADR value to determine the duty cycle of the output waveform, and to decide whether to output a fine-adjustment pulse equal in width to the resolution. To enable this operation, this register must be set within a range that depends on the CFS bit. If the DADR value is outside this range, the PWM output is held constant. A channel can be operated with 12-bit precision by fixing DA0 and DA1 to 0. The two data bits are not compared with UC12 and UC13 of DACNT.
1	CFS	1	R/W	Carrier Frequency Select 0: Base cycle = resolution (T) · 64 The range of DA13 to DA0: H'0100 to H'3FFF 1: Base cycle = resolution (T) · 256 The range of DA13 to DA0: H'0040 to H'3FFF
0		1	R	Reserved This bit is always read as 1 and cannot be modified.

DADRB

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	DA13 to DA0	All 1	R/W	D/A Data 13 to 0 These bits set a digital value to be converted to an analog value. In each base cycle, the DACNT value is continually compared with the DADR value to determine the duty cycle of the output waveform, and to decide whether to output a fine-adjustment pulse equal in width to the resolution. To enable this operation, this register must be set within a range that depends on the CFS bit. If the DADR value is outside this range, the PWM output is held constant. A channel can be operated with 12-bit precision by fixing DA0 and DA1 to 0. The two data bits are not compared with UC12 and UC13 of DACNT.
1	CFS	1	R/W	Carrier Frequency Select 0: Base cycle = resolution (T) · 64 DA13 to DA0 range = H'0100 to H'3FFF 1: Base cycle = resolution (T) · 256 DA13 to DA0 range = H'0040 to H'3FFF
0	REGS	1	R/W	Register Select DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. When changing the register to be accessed, set this bit in advance. 0: DADRA and DADRB can be accessed 1: DACR and DACNT can be accessed

10.3.3 PWMX (D/A) Control Register (DACR)

DACR enables the PWM outputs, and selects the output phase and operating speed.

Bit	Bit Name	Initial Value	R/W	Description
7		0	R/W	Reserved The initial value should not be changed.
6	PWME	0	R/W	PWMX Enable Starts or stops the PWM D/A counter (DACNT). 0: DACNT operates as a 14-bit up-counter 1: DACNT halts at H'0003
5, 4		All 1	R	Reserved These bits are always read as 1 and cannot be modified.
3	OEB	0	R/W	Output Enable B Enables or disables output on PWMX (D/A) channel B. 0: PWMX (D/A) channel B output (at the PWX1, PWX3 pins) is disabled 1: PWMX (D/A) channel B output (at the PWX1, PWX3 pins) is enabled
2	OEA	0	R/W	Output Enable A Enables or disables output on PWMX (D/A) channel A. 0: PWMX (D/A) channel A output (at the PWX0, PWX2 pin) is disabled 1: PWMX (D/A) channel A output (at the PWX0, PWX2 pins) is enabled
1	OS	0	R/W	Output Select Selects the phase of the PWMX (D/A) output. 0: Direct PWMX (D/A) output 1: Inverted PWMX (D/A) output
0	CKS	0	R/W	Clock Select Selects the PWMX (D/A) resolution. Eight kinds of resolution can be selected. 0: Operates at resolution (T) = system clock cycle time (t_{cyc}) 1: Operates at resolution (T) = system clock cycle time (t_{cyc}) · 2, · 64, · 128, · 256, · 1024, · 4096, and · 16384.

10.3.4 Peripheral Clock Select Register (PCSR)

PCSR and the CKS bit of DACR select the operating speed.

Bit	Bit Name	Initial Value	R/W	Description
7	PWCKX1B	0	R/W	PWMX_1 Clock Select
6	PWCKX1A	0	R/W	These bits select a clock cycle with the CKS bit of DACR of PWMX_1 being 1. See table 10.2.
5	PWCKX0B	0	R/W	PWMX_0 Clock Select
4	PWCKX0A	0	R/W	These bits select a clock cycle with the CKS bit of DACR of PWMX_0 being 1. See table 10.2.
3	PWCKX1C	0	R/W	PWMX_1 Clock Select This bit selects a clock cycle with the CKS bit of DACR of PWMX_1 being 1. See table 10.2.
2	PWCKB	0	R/W	PWM Clock Select B and A
1	PWCKA	0	R/W	See section 9.3.5, Peripheral Clock Select Register (PCSR).
0	PWCKX0C	0	R/W	PWMX_0 Clock Select This bit selects a clock cycle with the CKS bit of DACR of PWMX_0 being 1. See table 10.2.

Table 10.2 Clock Select of PWMX_1 and PWMX_0

PWCKX0C PWCKX1C	PWCKX0B PWCKX1B	PWCKX0A PWCKX1A	Resolution (T)
0	0	0	Operates on the system clock cycle (t_{cyc}) x 2
0	0	1	Operates on the system clock cycle (t_{cyc}) x 64
0	1	0	Operates on the system clock cycle (t_{cyc}) x 128
0	1	1	Operates on the system clock cycle (t_{cyc}) x 256
1	0	0	Operates on the system clock cycle (t_{cyc}) x 1024
1	0	1	Operates on the system clock cycle (t_{cyc}) x 4096
1	1	0	Operates on the system clock cycle (t_{cyc}) x 16384
1	1	1	Setting prohibited

10.4 Bus Master Interface

DACNT, DADRA, and DADRB are 16-bit registers. The data bus linking the bus master and the on-chip peripheral modules, however, is only 8 bits wide. When the bus master accesses these registers, it therefore uses an 8-bit temporary register (TEMP).

These registers are written to and read from as follows.

Write
When the upper byte is written to, the upper-byte write data is stored in TEMP. Next, when the lower byte is written to, the lower-byte write data and TEMP value are combined, and the combined 16-bit value is written in the register.

Read
When the upper byte is read from, the upper-byte value is transferred to the CPU and the lower-byte value is transferred to TEMP. Next, when the lower byte is read from, the lower-byte value in TEMP is transferred to the CPU.

These registers should always be accessed 16 bits at a time with a MOV instruction, and the upper byte should always be accessed before the lower byte. Correct data will not be transferred if only the upper byte or only the lower byte is accessed. Also note that a bit manipulation instruction cannot be used to access these registers.

Example 1: Write to DACNT

```
MOV.W R0, @DACNT        ; Write R0 contents to DACNT
```

Example 2: Read DADRA

```
MOV.W @DADRA, R0        ; Copy contents of DADRA to R0
```

10.5 Operation

A PWM waveform like the one shown in figure 10.2 is output from the PWX pin. DA13 to DA0 in DADR corresponds to the total width (T_L) of the low (0) pulses output in one conversion cycle (256 pulses when CFS = 0, 64 pulses when CFS = 1). When OS = 0, this waveform is directly output. When OS = 1, the output waveform is inverted, and DA13 to DA0 in DADR value corresponds to the total width (T_H) of the high (1) output pulses. Figures 10.3 and 10.4 show the types of waveform output available.

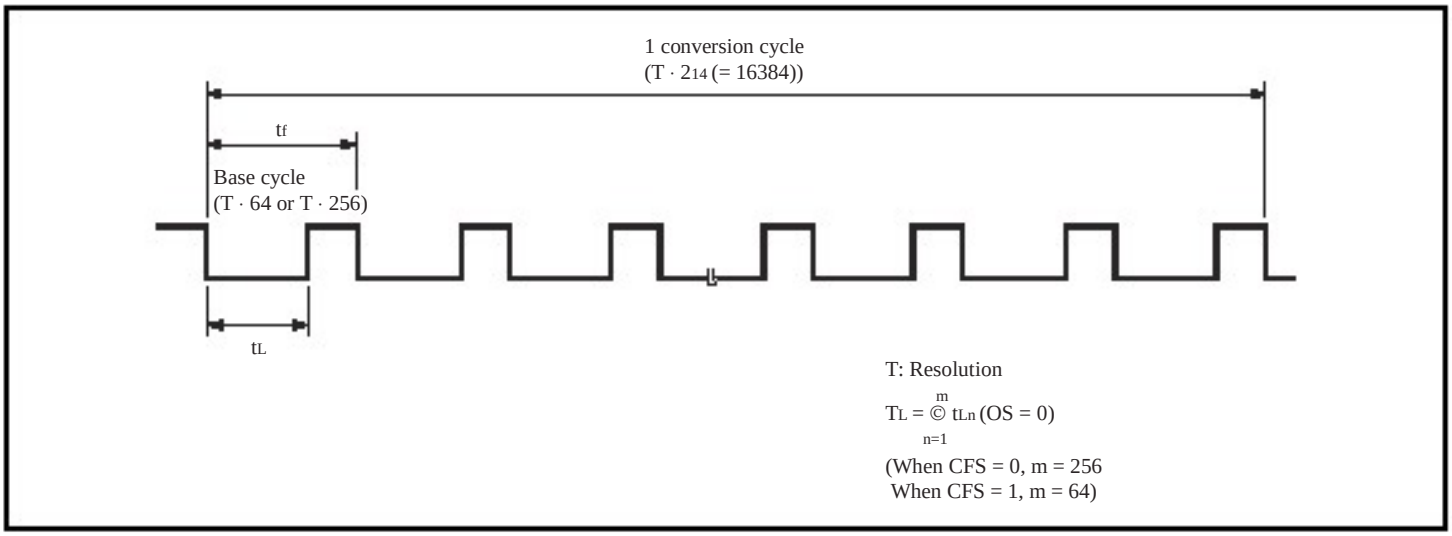


Figure 10.2 PWMX (D/A) Operation

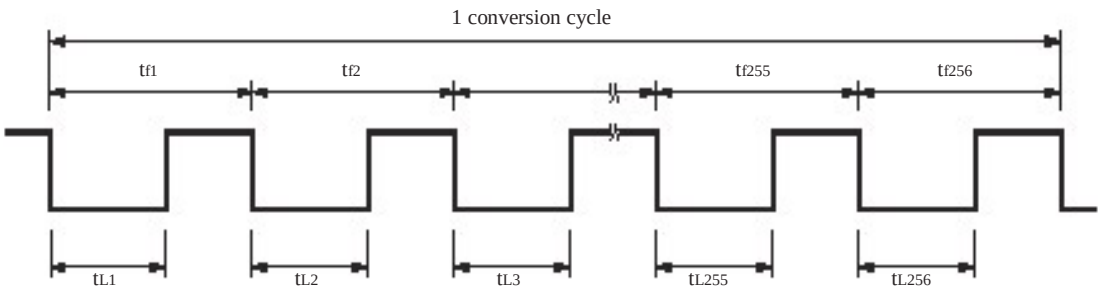
Table 10.3 summarizes the relationships between the CKS and CFS bit settings and the resolution, base cycle, and conversion cycle. The PWM output remains fixed unless DA13 to DA0 in DADR contain at least a certain minimum value. The relationship between the OS bit and the output waveform is shown in figures 10.3 and 10.4.

Table 10.3 Settings and Operation (Examples when ⎫ = 33 MHz)

PCSR									Fixed DADR Bits					
PWCKX0 / PWCKX1				Reso-lution T		Base	Conver-sion			Bit Data				Conversion
C	B	A	CKS	(µs)	CFS	Cycle	Cycle	TL/TH (OS = 0/OS = 1)	Accuracy (Bits)	DA3	DA2	DA1	DA0	Cycle (ms)*
⎪⎪		⎪	0	0.03	0	1.94	496.48	Always low/high output	14					0.50
						(µs)	(µs)	DA13 to 0 = H'0000 to H'00FF	12			0	0	0.12
								(Data value) · T						
						/515.6kHz		DA13 to 0 = H'0100 to H'3FFF	10	0	0	0	0	0.03
					1	7.76	496.48	Always low/high output	14					0.50
						(µs)	(µs)	DA13 to 0 = H'0000 to H'003F	12			0	0	0.12
								(Data value) · T						
				(φ)		/128.9kHz		DA13 to 0 = H'0040 to H'3FFF	10	0	0	0	0	0.03
0	0	0	1	0.06	0	3.88	0.99	Always low/high output	14					0.99
						(µs)	(ms)	DA13 to 0 = H'0000 to H'00FF	12			0	0	0.25
								(Data value) · T						
						/257.8kHz		DA13 to 0 = H'0100 to H'3FFF	10	0	0	0	0	0.06
					1	15.52	0.99	Always low/high output	14					0.99
						(µs)	(ms)	DA13 to 0 = H'0000 to H'003F	12			0	0	0.25
								(Data value) · T						
				(φ/2)		/64.5kHz		DA13 to 0 = H'0040 to H'3FFF	10	0	0	0	0	0.06
0	0	1	1	1.94	0	124.12	31.78	Always low/high output	14					31.78
						(µs)	(ms)	DA13 to 0 = H'0000 to H'00FF	12			0	0	7.94
								(Data value) · T						
						/8.1kHz		DA13 to 0 = H'0100 to H'3FFF	10	0	0	0	0	1.99
					1	496.48	31.78	Always low/high output	14					31.78
						(µs)	(ms)	DA13 to 0 = H'0000 to H'003F	12			0	0	7.94
								(Data value) · T						
				(φ/64)		/2.0kHz		DA13 to 0 = H'0040 to H'3FFF	10	0	0	0	0	1.99
0	1	0	1	3.88	0	248.24	63.55	Always low/high output	14					63.55
						(µs)	(ms)	DA13 to 0 = H'0000 to H'00FF	12			0	0	15.89
								(Data value) · T						
						/4.0kHz		DA13 to 0 = H'0100 to H'3FFF	10	0	0	0	0	3.97
					1	992.97	63.55	Always low/high output	14					63.55
						(µs)	(ms)	DA13 to 0 = H'0000 to H'003F	12			0	0	15.89
								(Data value) · T						
				(φ/128)		/1.0kHz		DA13 to 0 = H'0040 to H'3FFF	10	0	0	0	0	3.97

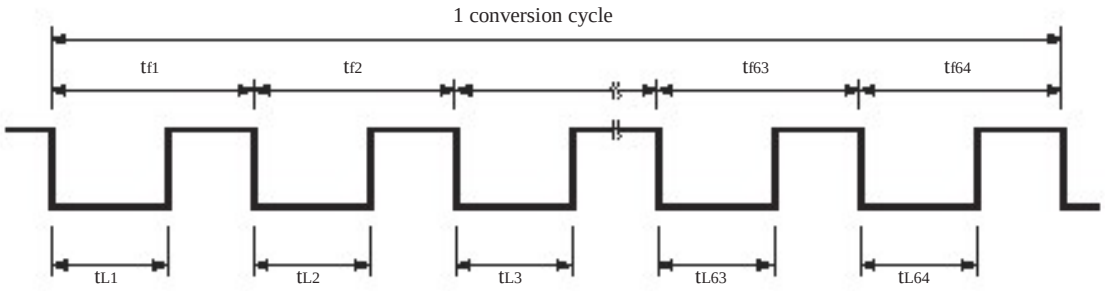
PCSR									Fixed DADR Bits					
PWCKX0 PWCKX1				Reso-lution T		Base	Conver-sion	TL/TH	Accuracy	Bit Data				Conversion
C	B	A	CKS (µs)		CFS	Cycle	Cycle	(OS = 0/OS = 1)	(Bits)	DA3	DA2	DA1	DA0	Cycle (ms)*
0	1	1	1	7.76	0	496.48	127.10	Always low/high output	14					127.10
						(µs)	(ms)	DA13 to 0 = H'0000 to H'00FF	12			0	0	31.78
						/2.0kHz		(Data value) · T	10	0	0	0	0	7.94
								DA13 to 0 = H'0100 to H'3FFF						
					1	1985.94	127.10	Always low/high output	14					127.10
						(µs)	(ms)	DA13 to 0 = H'0000 to H'003F	12			0	0	31.78
				(φ/256)		/0.5kHz		(Data value) · T	10	0	0	0	0	7.94
								DA13 to 0 = H'0040 to H'3FFF						
1	0	0	1	31.03	0	1.99	508.40	Always low/high output	14					508.40
						(ms)	(ms)	DA13 to 0 = H'0000 to H'00FF	12			0	0	127.10
						/503.5Hz		(Data value) · T	10	0	0	0	0	31.78
								DA13 to 0 = H'0100 to H'3FFF						
					1	7.94	508.40	Always low/high output	14					508.40
						(ms)	(ms)	DA13 to 0 = H'0000 to H'003F	12			0	0	127.10
				(φ/1024)		/125.9Hz		(Data value) · T	10	0	0	0	0	31.78
								DA13 to 0 = H'0040 to H'3FFF						
1	0	1	1	124.12	0	7.94	2.03	Always low/high output	14					2033.60
						(ms)	(s)	DA13 to 0 = H'0000 to H'00FF	12			0	0	508.40
						/125.9Hz		(Data value) · T	10	0	0	0	0	127.10
								DA13 to 0 = H'0100 to H'3FFF						
					1	31.78	2.03	Always low/high output	14					2033.60
						(ms)	(s)	DA13 to 0 = H'0000 to H'003F	12			0	0	508.40
				(φ/4096)		/31.5Hz		(Data value) · T	10	0	0	0	0	127.10
								DA13 to 0 = H'0040 to H'3FFF						
1	1	0	1	496.48	0	31.78	8.13	Always low/high output	14					8134.41
						(ms)	(s)	DA13 to 0 = H'0000 to H'00FF	12			0	0	2033.60
						/31.5Hz		(Data value) · T	10	0	0	0	0	508.40
								DA13 to 0 = H'0100 to H'3FFF						
					1	127.10	8.13	Always low/high output	14					8134.41
						(ms)	(s)	DA13 to 0 = H'0000 to H'003F	12			0	0	2033.60
				(φ/16384)		/7.9Hz		(Data value) · T	10	0	0	0	0	508.40
								DA13 to 0 = H'0040 to H'3FFF						
1	1	1	1	Setting prohibited										

Note: * Indicates the conversion cycle when specific DA3 to DA0 bits are fixed.



$t_{f1} = t_{f2} = t_{f3} = \cdots = t_{f255} = t_{f256} = T \times 64$
$t_{L1} + t_{L2} + t_{L3} + \cdots + t_{L255} + t_{L256} = T_L$

a. CFS = 0 [base cycle = resolution (T) · 64]



$t_{f1} = t_{f2} = t_{f3} = \cdots = t_{f63} = t_{f64} = T \times 256$
$t_{L1} + t_{L2} + t_{L3} + \cdots + t_{L63} + t_{L64} = T_L$

b. CFS = 1 [base cycle = resolution (T) · 256]

Figure 10.3 Output Waveform (OS = 0, DADR corresponds to T_L)

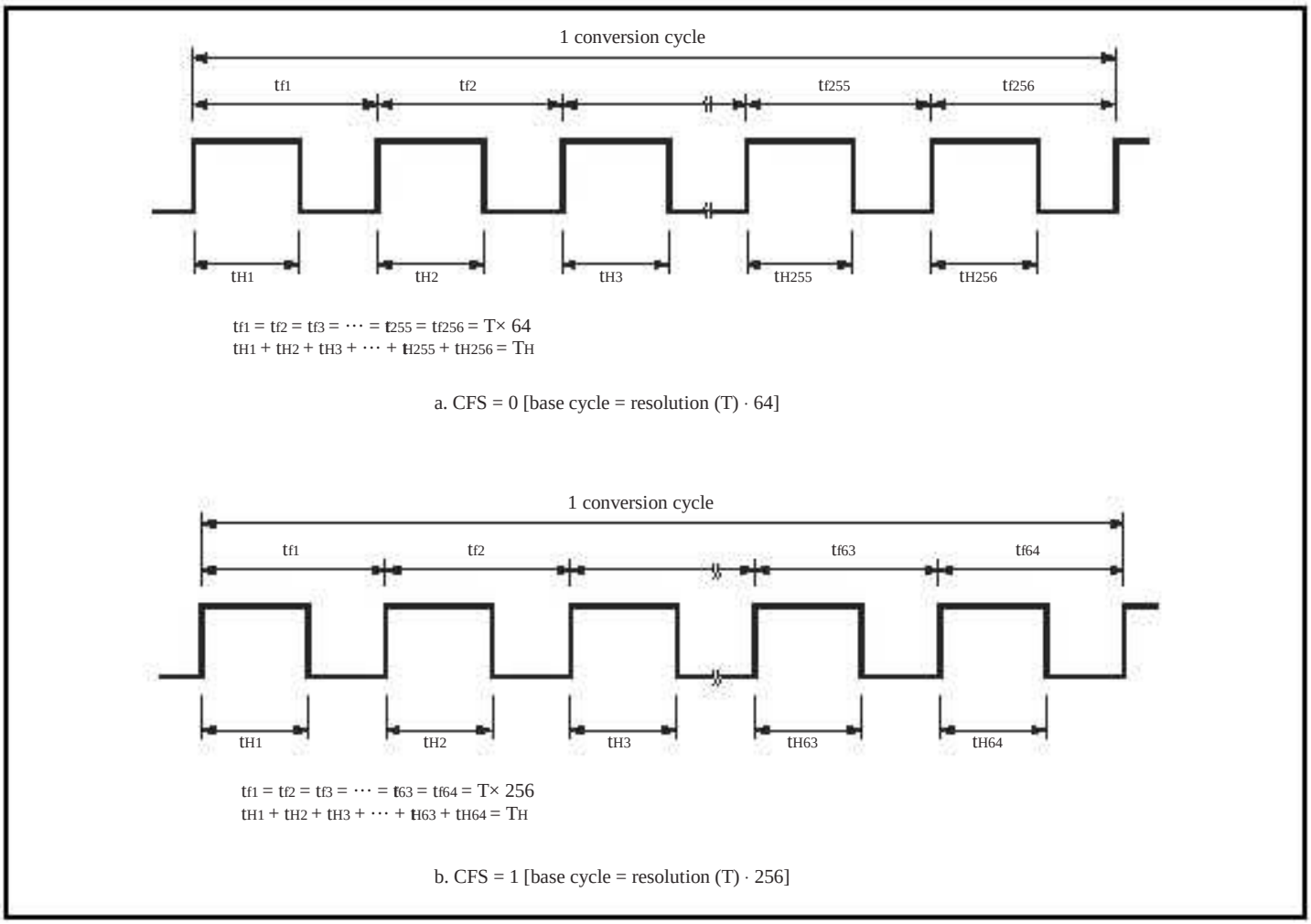


Figure 10.4 Output Waveform (OS = 1, DADR corresponds to T_H)

An example of the additional pulses when CFS = 1 (base cycle = resolution (T) · 256) and OS = 1 (inverted PWM output) is described below. When CFS = 1, the upper eight bits (DA13 to DA6) in DADR determine the duty cycle of the base pulse while the subsequent six bits (DA5 to DA0) determine the locations of the additional pulses as shown in figure 10.5.

Table 10.4 lists the locations of the additional pulses.

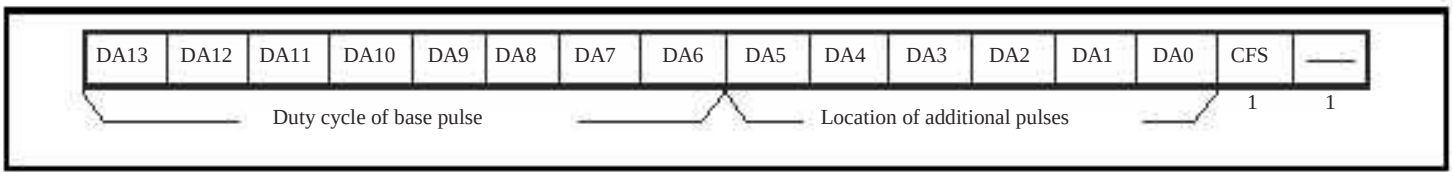


Figure 10.5 D/A Data Register Configuration when CFS = 1

In this example, DADR = H'0207 (B'0000 0010 0000 0111). The output waveform is shown in figure 10.6. Since CFS = 1 and the value of the upper eight bits is B'0000 0010, the high width of the base pulse duty cycle is 2/256 · (T).

Since the value of the subsequent six bits is B'0000 01, an additional pulse is output only at the location of base pulse No. 63 according to table 10.4. Thus, an additional pulse of 1/256 · (T) is to be added to the base pulse.

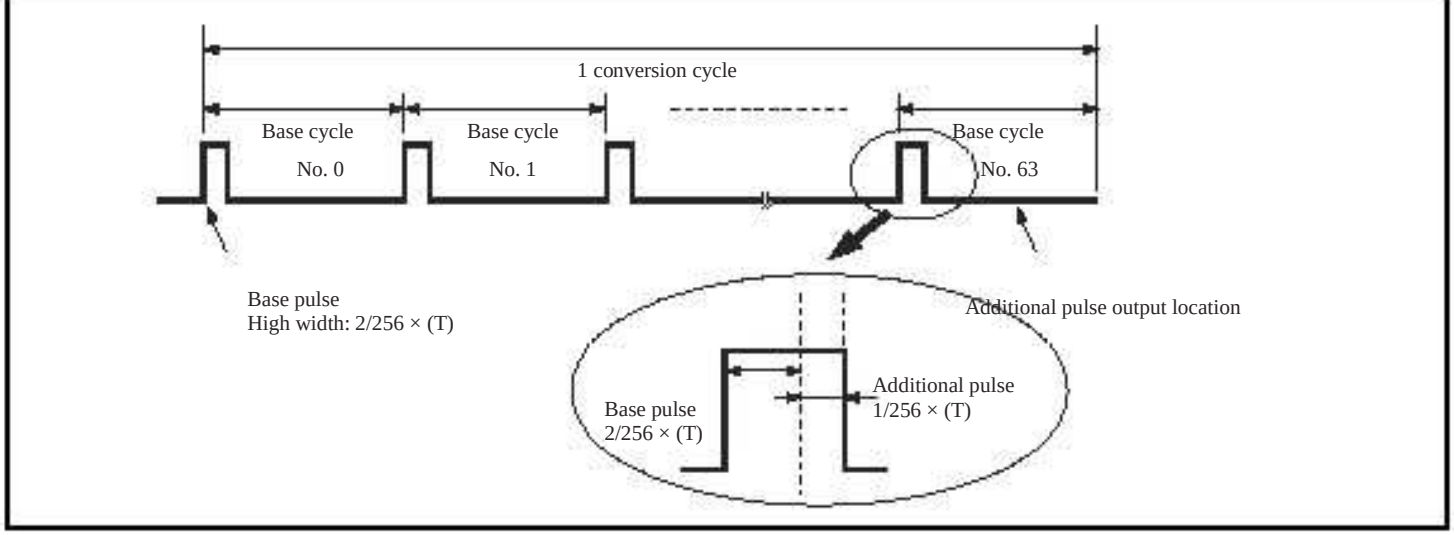


Figure 10.6 Output Waveform when DADR = H'0207 (OS = 1)

However, when CFS = 0 (base cycle = resolution (T) · 64), the duty cycle of the base pulse is determined by the upper six bits and the locations of the additional pulses by the subsequent eight bits with a method similar to as above.

Table 10.4 Locations of Additional Pulses Added to Base Pulse (When CFS = 1)