EE 382M (#16675)
VLSI I

Spring 2009

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Electrical and Computer Engineering
The University of Texas at Austin

Goals of this Course

- Learn to design and synthesize state-of-the-art digital Very Large Scale Integrated (VLSI) chips using CMOS technology
- Employ hierarchical design methods
  - Use integrated circuit cells as building blocks
  - Understand design issues at the layout, transistor, logic and register-transfer levels
- Use commercial design software in the lab
- **Understand the complete design flow**
- **Be able to design state-of-the-art CMOS chips in industry**

Course Information

- Class meets Tue/Thu, 12:30–2:00, RLM 5.112
  - **Discussion sessions on some Fridays (on lab and homework assignments)**
  - **Lab/TA hours posted at class web site**
- Instructor: David Z. Pan
  - ACES 5.434. (512) 471-1436, dpan@ece.utexas.edu
  - Office hours: Tue/Thu 3-4pm or by appointment
- Course Web Pages:

  http://users.ece.utexas.edu/~dpan/2009Spring_EE382M/ee382m_index.htm

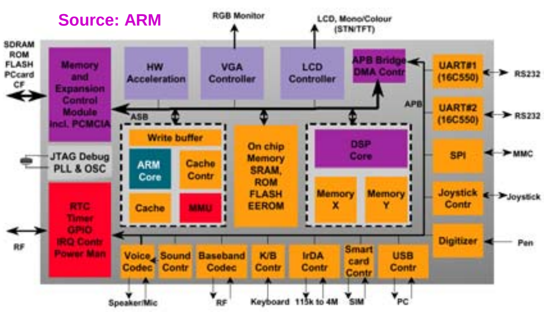
Acknowledgements
- J. Abraham (UT), A. Aziz (UT), D. Harris (HMC), R. Tupuri (AMD)

Course Information, Cont'd

- Prerequisites: logic design, basic computer organization
- Textbook: Weste and Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison Wesley/Pearson, 3rd Edition, 2005
- Lectures and discussion in class will cover basics of course
- Homework, Laboratory exercises will help you gain a deep understanding of the subject

Example System-on-a-Chip (SoC) for Mobile Applications

Source: ARM



A Brief History of the Transistor

Some of the events which led to the microprocessor

- Photographs in the following are from "State of the Art: A photographic history of the integrated circuit", Stan Augarten, Ticknor & Fields, 1983.

- They can also be viewed on the Smithsonian web site http://smithsonianchips.si.edu/

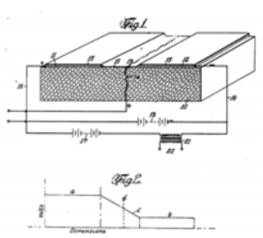
- Another web site http://www.pbs.org/transistor/

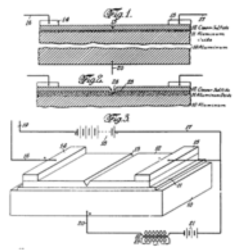
Early Ideas Leading to the Transistor

- J. W. Lilienfeld's patents

1930: "Method and apparatus for controlling electric currents", U.S. Patent 1,745,175

1933: "Device for controlling electric current", U. S. Patent 1,900,018

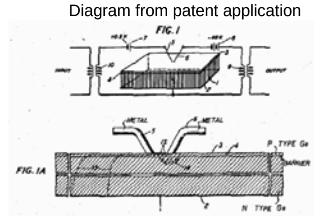


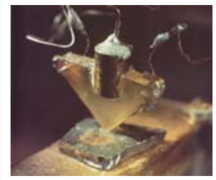


Key Developments at Bell Labs

- 1940: Ohl develops the PN Junction
- 1945: Shockley's laboratory established
- 1947: Bardeen and Brattain create point contact transistor (U.S. Patent 2,524,035)

Diagram from patent application

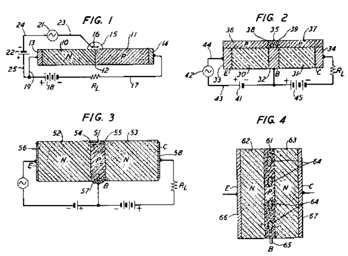




Developments at Bell Labs, Cont'd

- 1951: Shockley develops a junction transistor manufacturable in quantity (U.S. Patent 2,623,105)

Diagram from patent application



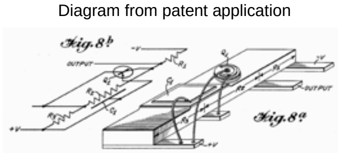
1950s – Silicon Valley

- 1950s: Shockley in Silicon Valley
- 1955: Noyce joins Shockley Laboratories
- 1954: The first transistor radio
- 1957: Noyce leaves Shockley Labs to form Fairchild with Jean Hoerni and Gordon Moore
- 1958: Hoerni invents technique for diffusing impurities into Si to build planar transistors using a SiO_2 insulator
- 1959: Noyce develops first true IC using planar transistors, back-to-back PN junctions for isolation, diode-isolated Si resistors and SiO_2 insulation with evaporated metal wiring on top

The Integrated Circuit (IC)

- 1959: Jack Kilby, working at TI, dreams up the idea of a monolithic "integrated circuit"
  - Components connected by hand-soldered wires and isolated by "shaping", PN-diodes used as resistors (U.S. Patent 3,138,743)

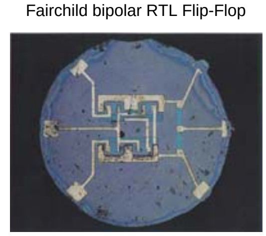
Diagram from patent application



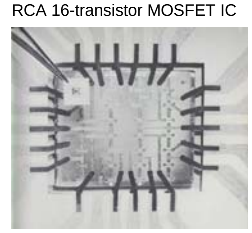
ICs, Cont'd

- 1961: TI and Fairchild introduce the first logic ICs ($50 in quantity)
- 1962: RCA develops the first MOS transistor

Fairchild bipolar RTL Flip-Flop

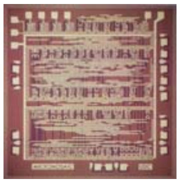


RCA 16-transistor MOSFET IC



Computer-Aided Design (CAD)

- 1967: Fairchild develops the “Micromosaic” IC using CAD
  - Final Al layer of interconnect could be customized for different applications



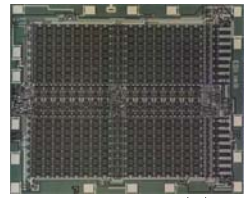
- 1968: Noyce, Moore leave Fairchild, start Intel

Static and Dynamic RAMs

- 1970: Fairchild introduces the 4100, 256-bit Static RAM
- 1970: Intel starts selling a1K-bit Dynamic RAM, the 1103

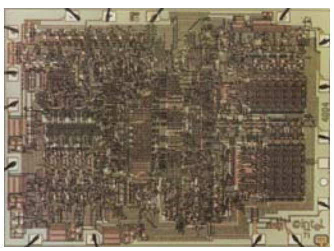
Fairchild 4100 256-bit SRAM

Intel 1103 1K-bit DRAM

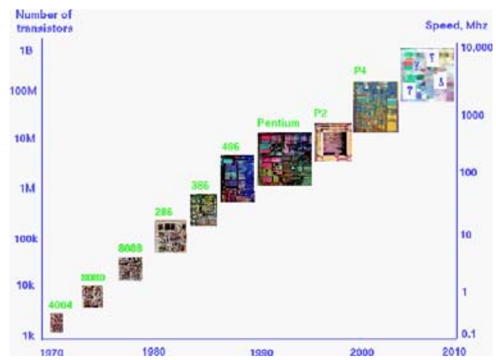


The Microprocessor!

- 1971: Intel introduces the first microprocessor, the 4004 (originally designed as a special circuit for a customer)



MOS Technology Trends



VLSI Design - The Big Picture

- What do you do with a billion transistors?
- **Important to identify potential applications**
- Designing systems for a particular application:
  - Identify sub-functions
  - **Design system using a variety of powerful Computer-Aided Design (CAD) tools**
- **Use a process relevant to industry**
  - **Work with industry leaders in Austin**

Circuit Design at UT

- UT leads in teaching and research
- Key Courses
  - VLSI Design
  - Advanced VLSI Design
  - Design of Systems on a Chip
  - Analog Design
- Electives
  - Physical design, nanometer scale, etc.
  - Data converters, RF IC Design, Integrated Sensors, etc.

Work in this Course

- Lectures
  - Read sections in text and slides before class
- Homework problems
  - Roughly 8 homeworks
- Laboratory exercises
  - Three major exercises dealing with various aspects of VLSI design
  - Complete each section before the deadline
- VLSI design project
  - Design an IP core, architecture to layout
- **Course involves a large amount of work throughout the semester**

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Types of IC Designs

- IC Designs can be **Analog** or **Digital**
- Digital designs can be one of three groups
- Full Custom
  - Every transistor designed and laid out by hand
- ASIC (Application-Specific Integrated Circuits)
  - Designs synthesized automatically from a high-level language description
- Semi-Custom
  - Mixture of custom and synthesized modules

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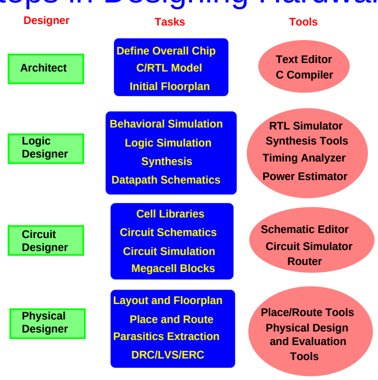
Steps in Designing Hardware



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Laboratory Exercises

- Lab Exercise 1
  - Design, layout and evaluation of a register file
    - Use Cadence layout software, HSpice simulation
- Lab Exercise 2
  - Design and evaluation of an ALU with standard cell libraries
    - Cadence schematic editor, Synopsys static timing analysis, Cadence place-and-route
- Lab Exercise 3
  - HDL level design and evaluation of bus controller
    - Synopsys simulation, Synopsys synthesis, Cadence place-and-route

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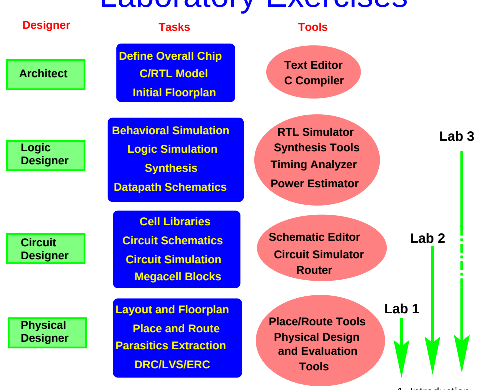
Laboratory Exercises



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Purpose of Lab Exercises

1. Familiarity with layout, circuit simulation, timing
2. Learn schematic design, timing optimization
3. Learn RT-level design, system simulation, logic synthesis and place-and-route

Using mix of tools from different vendors mirrors industry practice

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Laboratory Design Tools

- We will us commercial CAD tools
  - Cadence, Synopsys, etc.
- Commercial software is powerful, but very complex
  - Designers sent to long training classes
  - Students will benefit from using the software, but we don't have the luxury of long training
  - TAs have experience with the software
- Start work early in the lab
  - Unavailability of workstations is no excuse for late submissions
  - Plan designs carefully and save work frequently

Exams and Grading

- Two exams, in class, open book and notes
- Final Project

Weights for Final Grade:

Homework	10%
Exams	30%
Laboratory	35%
Final Proj.	25%

- Penalty for late submission: 5% per working day (maximum 25%, no submissions accepted after 5 working days)
- Bonus, early submission: 5%/working day (max 10%)

Academic Honesty

- **Cheating will not be tolerated!!!**
- Feel free to discuss homework, laboratory exercises with classmates, TAs and the instructors
- However, you should do the homework and lab exercises by yourself, **and the submitted work should be your own**
- We will check for cheating, and any incident will be reported to the department

What Will You Learn?

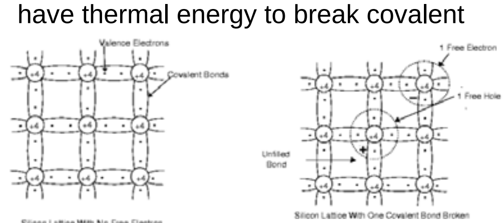
- How integrated circuits work
- How to design chips with millions of transistors
  - Ways of managing the complexity
  - Use of tools to speed up the design process
- Identifying performance bottlenecks
- Ways of speeding up circuits
- Making sure the designs are correct
- Making the chips testable after manufacture
- Other issues: effect of technologies, reducing power consumption, etc.

Learning General Principles

- Chip design involves optimization, tradeoffs
- Need the ability to work as part of a group
- Technology changes fast, so it is important to understand the general principles which would span technology generations
- Systems are implemented using building blocks (which may be technology-specific)
  - Example: relays → tubes → bipolar transistors → MOS transistors (which are like relay switches)
- **Lot of work in course, but you'll learn a lot**

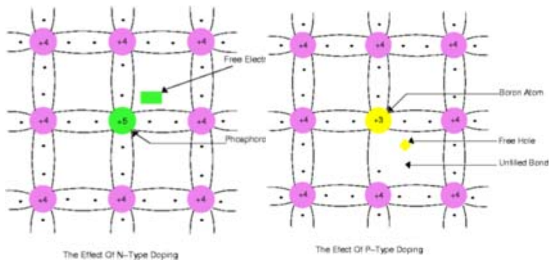
Conductivity in Silicon Lattice

- At temperatures close to 0º K, electrons in outermost shell tightly bound (insulator)
- At higher temps., (300º K), some electrons have thermal energy to break covalent



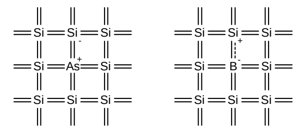
Conductivity in Semiconductors

- Pure Silicon may be mixed with **impurities** to change the number of available carriers



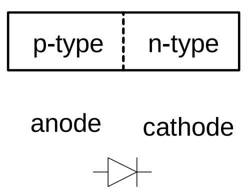
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



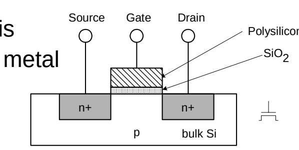
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



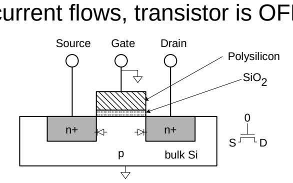
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



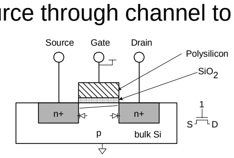
nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



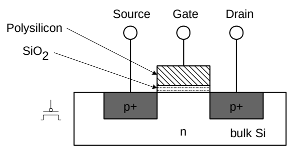
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

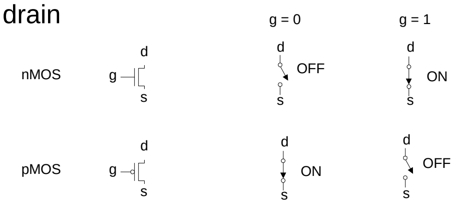


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

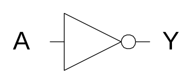
Transistors as Switches

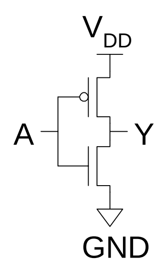
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

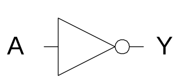
A	Y
0	
1	

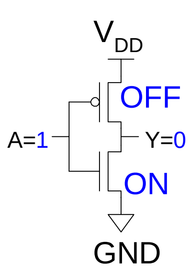




CMOS Inverter

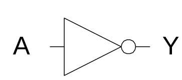
A	Y
0	
1	**0**

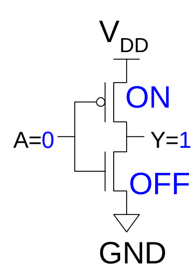




CMOS Inverter

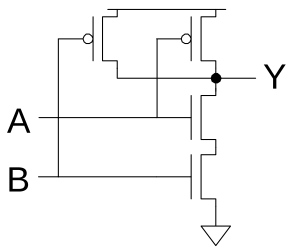
A	Y
0	**1**
1	0

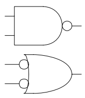




CMOS NAND Gate

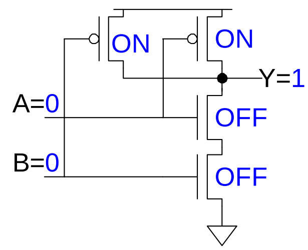
A	B	Y
0	0	
0	1	
1	0	
1	1	

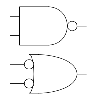




CMOS NAND Gate

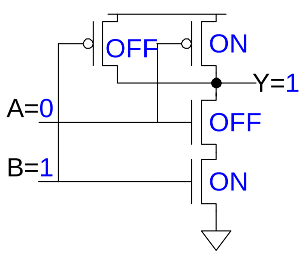
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

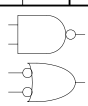




CMOS NAND Gate

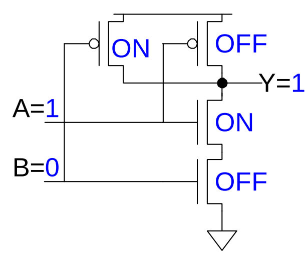
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

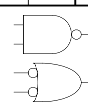




CMOS NAND Gate

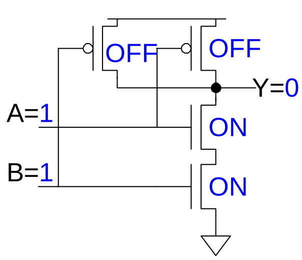
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

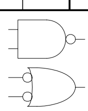




CMOS NAND Gate

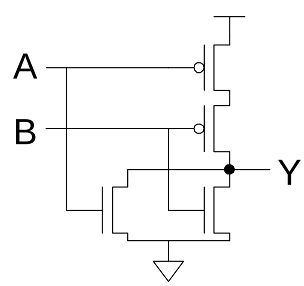
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

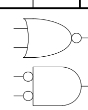




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



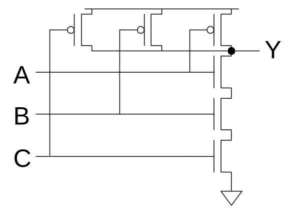


3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

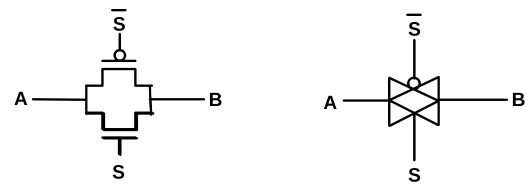


Characteristics of CMOS Gates

- In general, when the circuit is stable
  - There is a path from one supply (V_{SS} or V_{DD}) to the output (low static power dissipation)
  - There is NEVER a path from one supply to another
- There is a momentary drain of current when a gate switches from one state to the other
  - Dynamic power dissipation
- If a node has no path to power or ground, the previous value retained due to the capacitance of the node

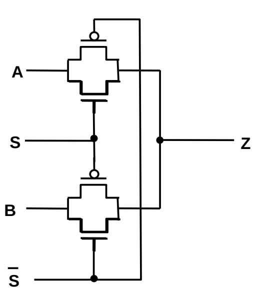
Complementary Switch (Transmission Gate)

- Combine n- and p-channel switches in parallel to get a switch which passes both "1" and "0" well



Multiplexer

- Two-input MUX using only switches



A	B	S	$\overline{S}$	Z	
X	0	0	1	0	B
X	1	0	1	1	
0	X	1	0	0	A
1	X	1	0	1	

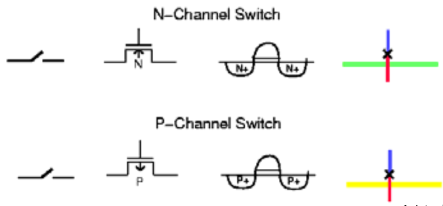
X: don't care

Schematic Vs. Physical Layout

- In schematic layout, lines drawn between device terminals represent connections
  - Any non-planar situation is dealt with by crossing lines
  - Provides more information than logic level (sizes of transistors, etc.)
- Physical layout captures interaction between layers
  - includes **diffusion**, **polysilicon**, **metal** (many layers of metal), **vias** (contacts)

Stick Diagram

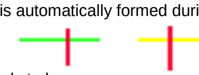
- Intermediate representation between the schematic level and the mask level
- Gives topological information (identifies different layers and their relationship)
  - Assumes that wires have no width



Basic Layers in CMOS

When two layers of the same material (i.e., on the same layer) touch or cross, they are connected and belong to the same electrical node

When Polysilicon crosses Diffusion (N or P), an N or P transistor is formed
There is no diffusion underneath the poly, but the diffusion must be drawn connecting the source and the drain
The self-aligned gate is automatically formed during fabrication



When a Metal line needs to be connected to a metal line on another layer, or to one of the other three conductors, a contact cut (via) is required