Introduction to CMOS VLSI Design

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Walla Walla College

Outline for Today

- ❑ Course organization
- ❑ History of the integrated circuit
- ❑ Trends in the semiconductor industry
- ❑ System design versus custom chip design
  - – Top down design
  - – Bottom-up implementation
  - – CAD tools

Course Objectives

- Learn to design and analyze state-of-the-art digital VLSI chips using CMOS technology
- Employ hierarchical design methods
  - Understand design issues at the layout, transistor, logic, and register-transfer levels
  - Use integrated circuit cells as building blocks
  - Use commercial design software in the lab
- Understand the complete design flow
  - Won't cover architecture, solid-state physics, analog design
  - Superficial treatment of transistor functioning

Course Topics

- Design methodology for large systems
- CAD tools and design processes (layout and simulation)
- Design rules
- MOS devices and IC Fabrication
- MOS circuit concepts
- Subsystem design
- MOS performance characteristics
- Testability

Course Information

- Instructor: Dr. Curtis Nelson
  - Phone: 527-2076
  - E-mail: nelscu@wwc.edu
  - Office: 263 Chan Shun Pavilion
- Class time: 11:00 MWF
- Lab time: 2:00 - 5:00pm Monday
- Course web page:
  http://people.wwc.edu/staff/nelscu/engr434/index.html
- Text book: Weste and Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, AW, 3rd edition

Prerequisites

- Logic design (engr354, *engr433*)
- Basic computer organization (cptr215, *cptr350*)
- Basic device electronics (engr356)
- Embedded systems (engr355)

Handouts

- There will be occasional handouts that extend or clarify material covered in the textbook. Unless stated otherwise, you are responsible for the content of these handouts.

Homework

- Homework is due at the start of class on the day specified. Homework that is late may suffer a penalty unless previous arrangements have been made with the instructor. Homework will likely not be accepted after that homework assignment has been graded and returned to the class. For proper format, see the homework guidelines posted on the course web page.

Project and Labs

- There will be a term project. Students will work in teams. The project details will be given to you at a later date.
- A sufficient number of Sun workstations are reserved for the class during this time. We will be using Mentor Graphics software and a new release of the analog design kit (ADK) on the Sun Blades. Note that you may use the Sun Ultras as xterms but you must run the software tools on one of the Blade machines. **CDE is the required desktop.**
- The Mentor Graphics tool set will be used
  - *Design Architect – IC* for schematic capture
  - *IC station* for layout
  - *Calibre* for analog and pseudo-digital simulation

Exams and Grading

- One midterm test

Weights for Final Grade

Homework	15%
Test	20%
Labs	25%
Project	40%

- The final grade will be based on the break points that usually occur when the final distribution for the entire class is ranked.

Other Information

- Please, no cell phones or other distracting objects in the classroom
- When absent, the student is responsible for obtaining information missed in class
- Any assignment made verbally is as binding as that which is written
- If you have a physical or learning disability and need accommodations please contact Sue Huett in the Teaching Learning Center, Village Hall, or call 2366. Accommodations for documented disabilities are arranged through the Disability Support Services (DSS) office. This syllabus and course materials are available in alternate format as appropriate to the disability . Accommodations are not retroactive. If you do not declare the disability to the DSS office, you may not receive appropriate accommodations.
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Work in the Course

- Lectures: mostly from text, not always in sequence
- Homework: 4-5 assignments
  - Mostly straightforward questions from the text
- Laboratory exercises
  - Labs 1-5: Custom IC design
  - Labs 6-10: Project related issues
- NOTE: This course involves a large amount of work

Laboratory Design Tools

- ❑ We will use commercial CAD
  - – Mentor Graphics and integrated tools
- ❑ Commercial software is powerful, but very complex
  - – Designers sent to long training classes
  - – Students will benefit from using the software, but we don't have the luxury of long training
  - – Your instructor (and some of you) have some experience with the software
- ❑ Start work early in the lab
  - – Plan designs carefully and save work frequently

Academic Honesty

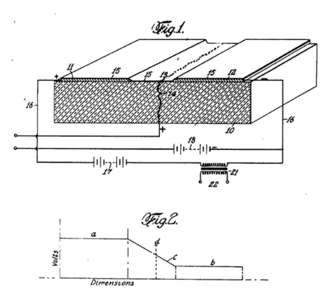
- ❑ Feel free to discuss homework, laboratory, and project exercises with classmates, lab assistant, and the instructor, However:
  - – Write the homework and lab exercises yourself

A Brief History of MOS

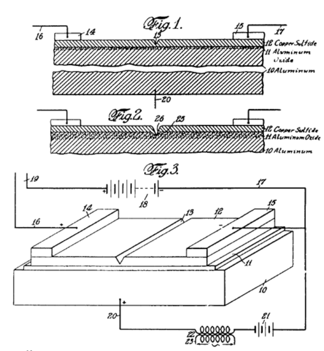
- The following slides portray some of the events which led to the microprocessor:
  - Photographs from “State of the Art: A photographic history of the integrated circuit,” Augarten, Ticknor, & Fields, 1983.
  - They can also be viewed on the Smithsonian web site, http://smithsonianchips.si.edu/

Lilienfeld Patents

1930: “Method and apparatus for controlling electric currents”, U.S. Patent 1,745,175



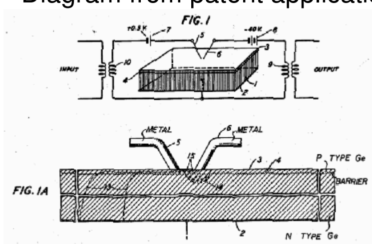
1933: “Device for controlling electric current”, U. S. Patent 1,900,018

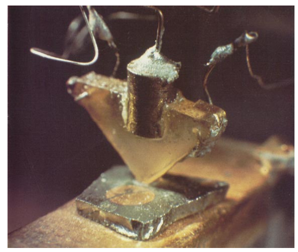


Bell Labs

- 1940: Ohl develops the PN Junction
- 1945: Shockley's laboratory established
- 1947: Bardeen and Brattain create point contact transistor (U.S. Patent 2,524,035)

Diagram from patent application



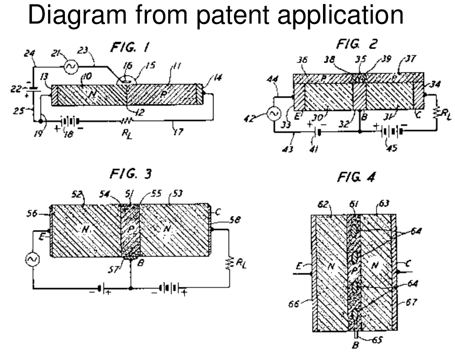


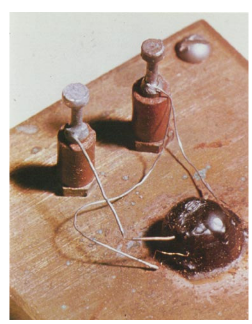
Introduction | CMOS VLSI Design | Slide 17

Bell Labs

- 1951: Shockley develops a junction transistor manufacturable in quantity (U.S. Patent 2,623,105)

Diagram from patent application





Introduction | CMOS VLSI Design | Slide 18

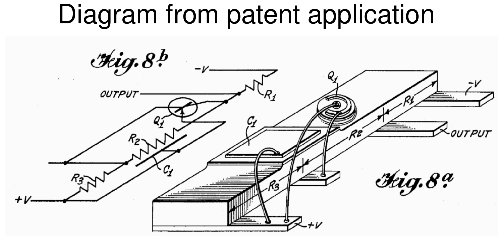
1950s – Silicon Valley

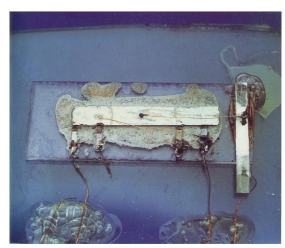
- 1950s: Shockley in Silicon Valley
- 1954: The first transistor radio
- 1955: Noyce joins Shockley Laboratories
- 1957: Noyce leaves Shockley Labs to form Fairchild with Jean Hoerni and Gordon Moore
- 1958: Hoerni invents technique for diffusing impurities into Si to build planar transistors using a SiO_2 insulator
- 1959: Noyce develops first true IC using planar transistors, back-to-back PN junctions for isolation, diode-isolated Si resistors, and SiO_2 insulation with evaporated metal wiring on top

The Integrated Circuit

- 1959: Jack Kilby, working at TI, dreams up the idea of a monolithic "integrated circuit"
  - Components connected by hand-soldered wires and isolated by "shaping", PN-diodes used as resistors (U.S. Patent 3,138,743)

Diagram from patent application

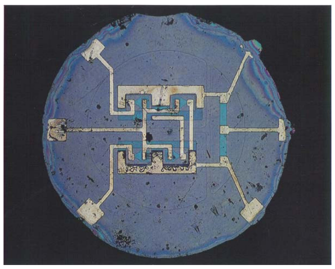




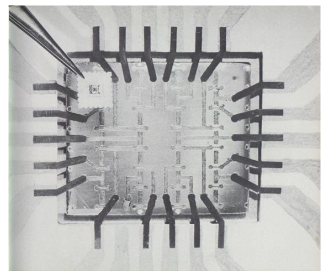
Integrated Circuits

- ❑ 1961: TI and Fairchild introduce the first logic ICs ($50 in quantity)
- ❑ 1962: RCA develops the first MOS transistor

Fairchild bipolar RTL Flip-Flop

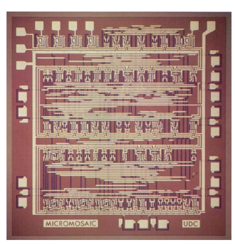


RCA 16-transistor MOSFET IC



Computer-Aided Design

- ❑ 1967: Fairchild develops the "Micromosaic" IC using CAD
  - – Final Aluminum layer of interconnect could be customized for different applications

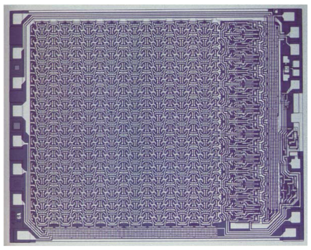


- ❑ 1968: Noyce, Moore leave Fairchild, start Intel

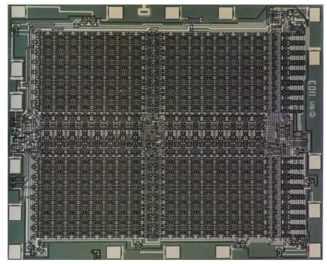
RAMs

- ❑ 1970: Fairchild introduces 256-bit Static RAMs
- ❑ 1970: Intel starts selling1K-bit Dynamic RAMs

Fairchild 4100 256-bit SRAM



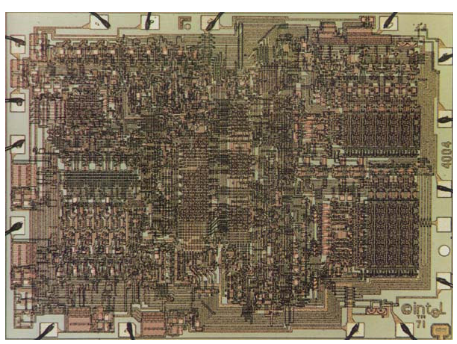
Intel 1103 1K-bit DRAM



Introduction CMOS VLSI Design Slide 23

The Microprocessor

- ❑ 1971: Intel introduces the 4004
  - – General purpose programmable computer



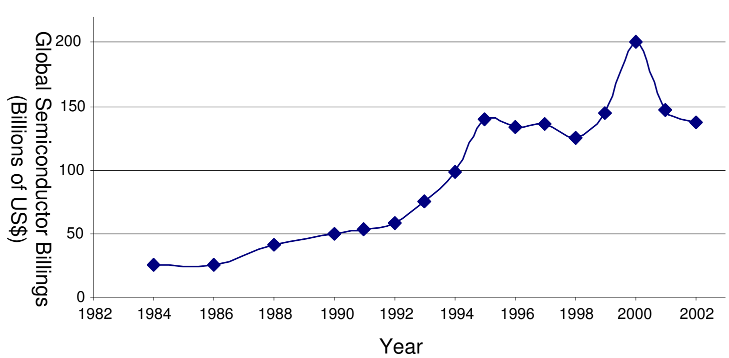
Introduction CMOS VLSI Design Slide 24

A Brief History

- 2003
  - Intel Pentium 4 μprocessor (55 million transistors)
  - 512 Mbit DRAM (> 0.5 billion transistors)
- 53% compound annual growth rate over 45 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power
  - Revolutionary effects on society

Annual Sales

- 10^{18} transistors manufactured in 2003
  - 100 million for every human on the planet

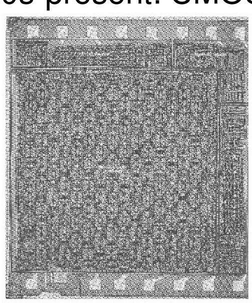


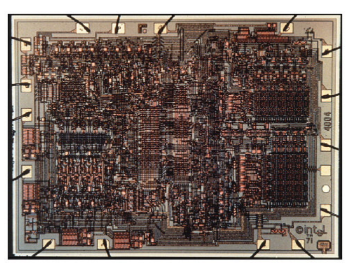
Transistor Types

- ❑ Bipolar transistors
  - – npn or pnp silicon structure
  - – Small current into very thin base layer controls large currents between emitter and collector
  - – Base currents limit integration density
- ❑ Metal Oxide Semiconductor Field Effect Transistors
  - – nMOS and pMOS MOSFETS
  - – Voltage applied to insulated gate controls current between source and drain
  - – Low power allows very high integration

MOS Integrated Circuits

- ❑ 1970's processes usually had only nMOS transistors
  - – Inexpensive, but consume power while idle
- ❑ 1980s-present: CMOS processes for low idle power

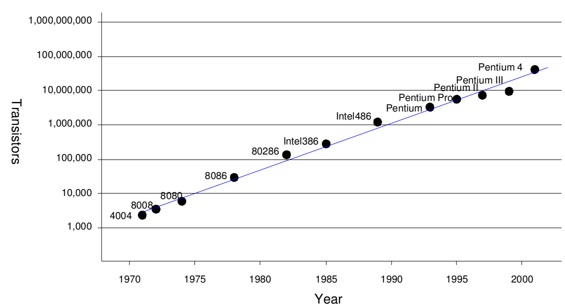




Intel 1101 256-bit SRAM Intel 4004 4-bit μP

Moore's Law

- 1965: Gordon Moore plotted transistor on each chip
  - Fit straight line on semi log scale
  - Transistor counts have doubled every 26 months



<u>Integration Levels</u>

SSI: 10 gates

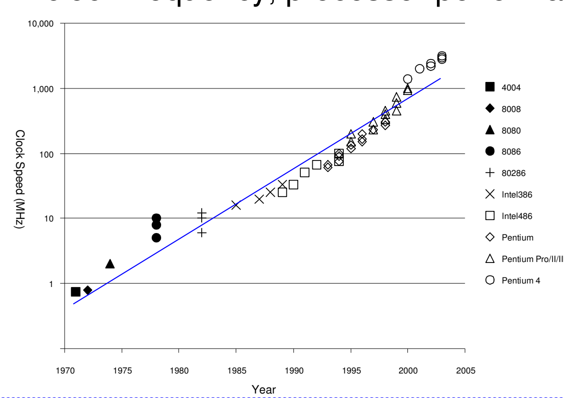
MSI: 1000 gates

LSI: 10,000 gates

VLSI: > 10k gates

Corollaries

- Many other factors grow exponentially
  - Ex: clock frequency, processor performance



Systems and Chips

- ❑ This course: designing ICs
  - Part of a system: chips + board + software + …
  - System companies: Dell, Cisco
  - Chip companies: Intel, Broadcom, AMD

Course Relevance

- ❑ 2003 world wide sales of chips: ~170B$
  - Primarily digital
  - High-margin business
  - Basis for systems
- ❑ Most computer engineering graduates work in
  - VLSI design: Intel
  - System design: Cisco
  - Software: Microsoft

What Will We Cover?

- ❑ Designing chips containing **lots** of transistors
  - – How basic components work (transistors, gates, flip-flops, memories, adders, etc)
  - – Complexity management: hierarchy and CAD tools
- ❑ Key issues
  - – Performance analysis and optimization
  - – Testing: functional and manufacturing
  - – Power consumption, clocking, I/O, etc

General Principles

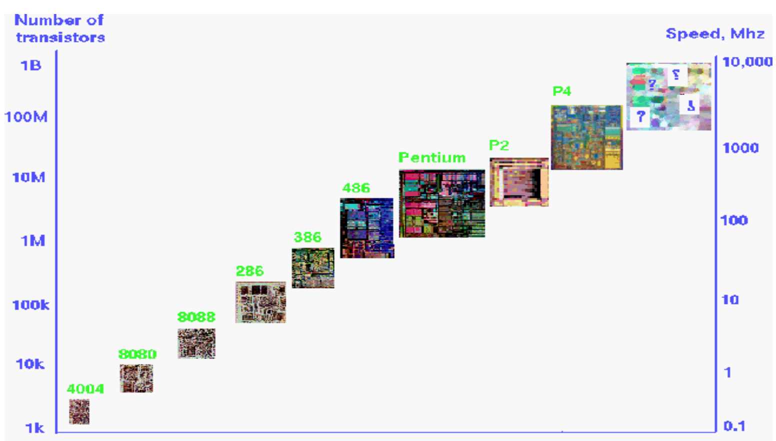
- ❑ Technology changes fast, so it is important to understand the general principles which span technology generations
  - – Optimization, tradeoffs
  - – Work as part of a group
  - – Leverage existing work: programs, building blocks
- ❑ Concepts remain the same
  - – Example: relays → tubes → bipolar transistors → MOS transistors → ???

Types of IC Designs

- ❑ IC Designs can be **Analog** or **Digital**
- ❑ Digital designs can be one of three groups
  - – Full Custom
    - Every transistor designed and laid out by hand
  - – ASIC (Application-Specific Integrated Circuits)
    - Designs synthesized automatically from a high-level language description
  - – Semi-Custom
    - Mixture of custom and synthesized modules

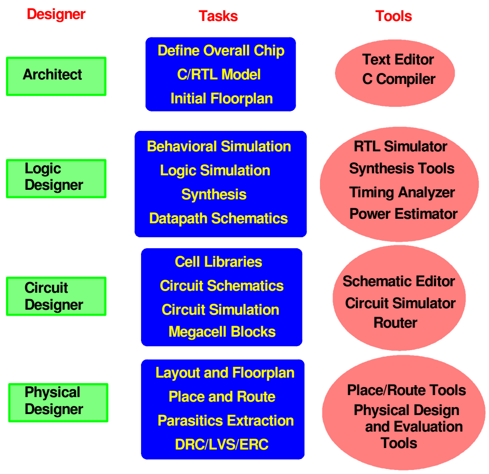
Introduction CMOS VLSI Design Slide 35

MOS Technology Trends



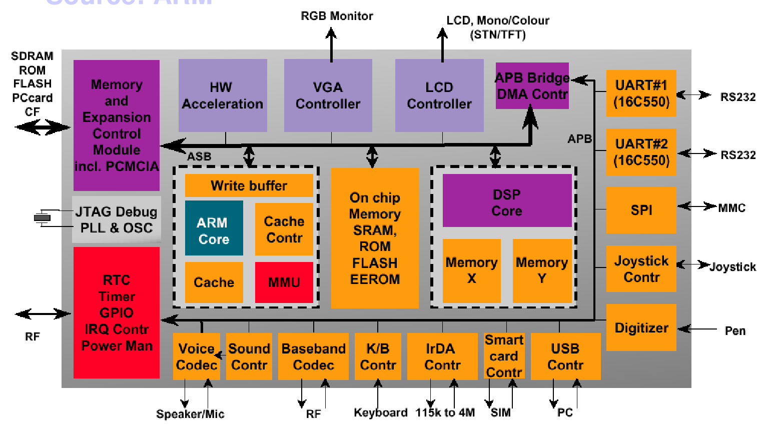
Introduction CMOS VLSI Design Slide 36

Steps in Design



System on a Chip

Source: ARM



Summary

- ❑ Presented the particulars of this course
- ❑ Covered the history of the integrated circuit
- ❑ Presented the trends in the semiconductor industry
- ❑ This course teaches both “bottom-up” and “top-down” design strategies