ASIC, Customer-Owned Tooling, and Processor Design

Design Style Myths That Lead EDA Astray

Nancy Nettleton
Manager, VLSI ASIC Device Engineering
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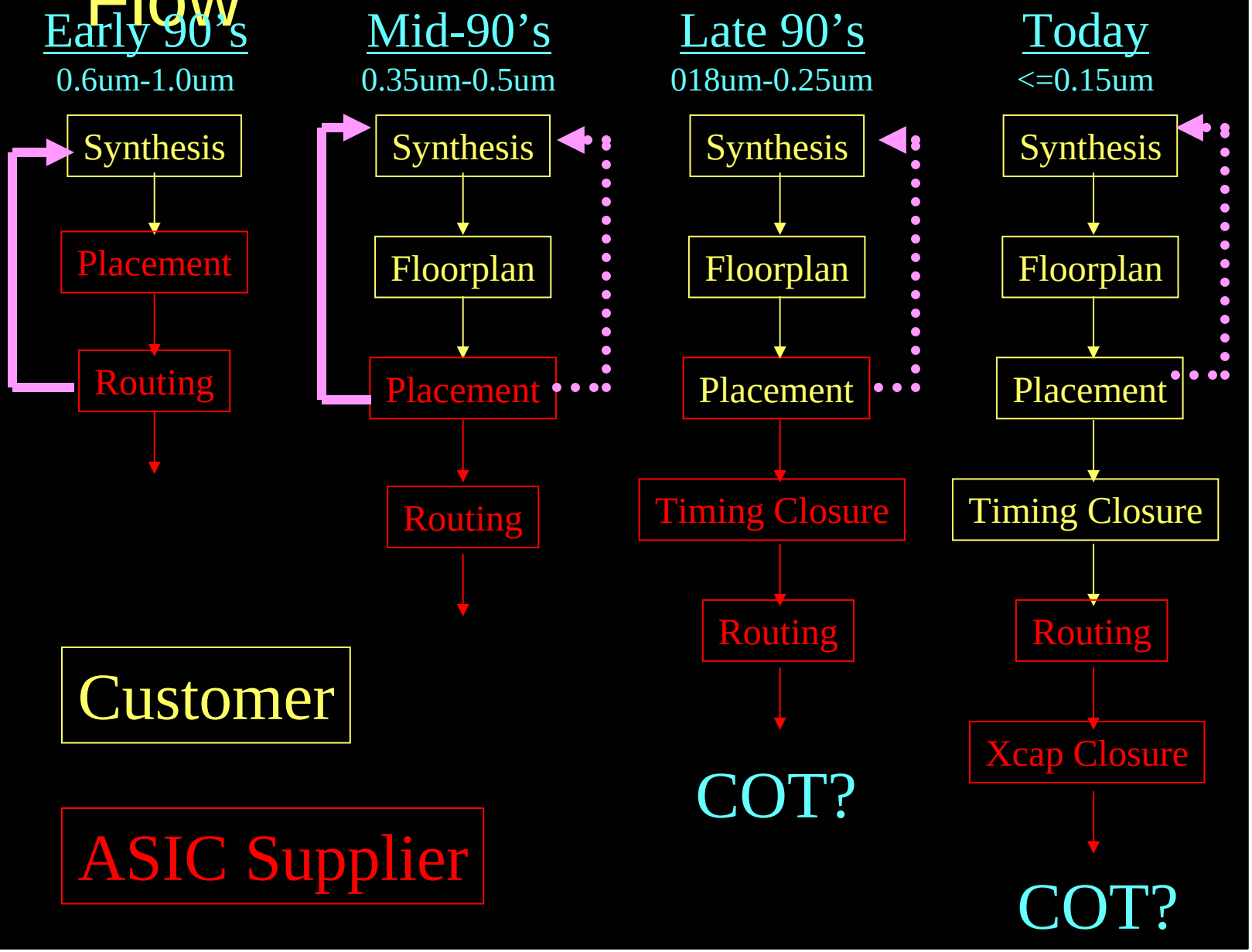
Design Style Myths

COT is a design style that achieves higher performance through greater ownership of physical design.

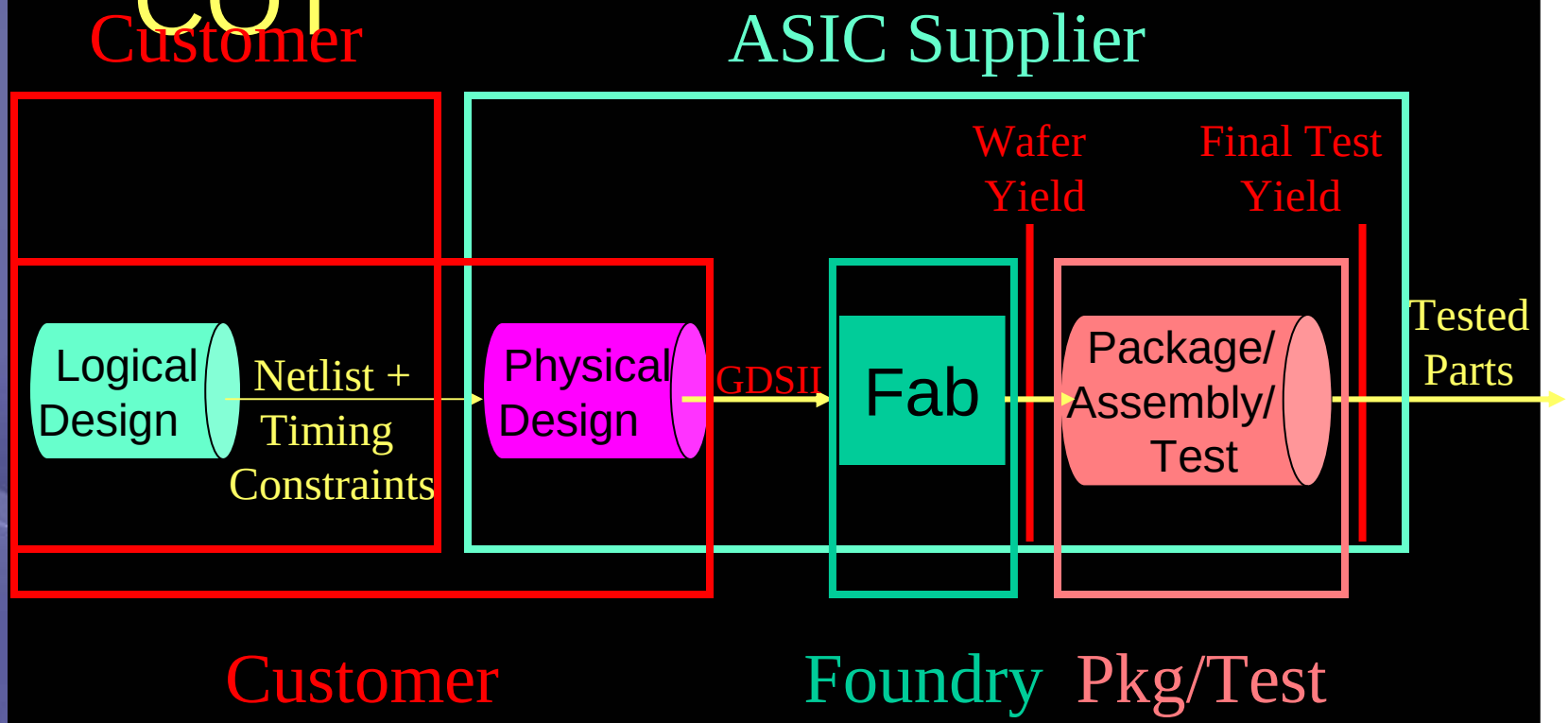
ASICs are slower than processors because of design margin.

Design automation tactics tuned on processors are effective on ASICs if they are more heavily automated.

Evolution of the ASIC Design Flow



Difference Between ASIC & COT



ASIC model: ASIC supplier responsible for physical design, silicon fabrication, & package/assembly/test.

COT model: Customer responsible for physical design, wafer, and final test yield.

Meaning of Customer-Owned Tooling Has Changed

- Used to mean who owned physical design, the foundry or the customer.
- Now it means who is responsible for the supply chain, regardless of the design flow used.
- The term *Customer-Owned Tooling*
  - No longer defines a design flow.
  - Transfer of silicon responsibility from a vertically integrated ASIC supplier to the customer (with commensurate cost reduction).

Implications of Yield Ownership

Two Types of Yield	ASIC Model	COT Model
Was the wafer processed correctly?	ASIC Supplier	Foundry
Was the design properly targeted within process distribution?	ASIC Supplier	Customer

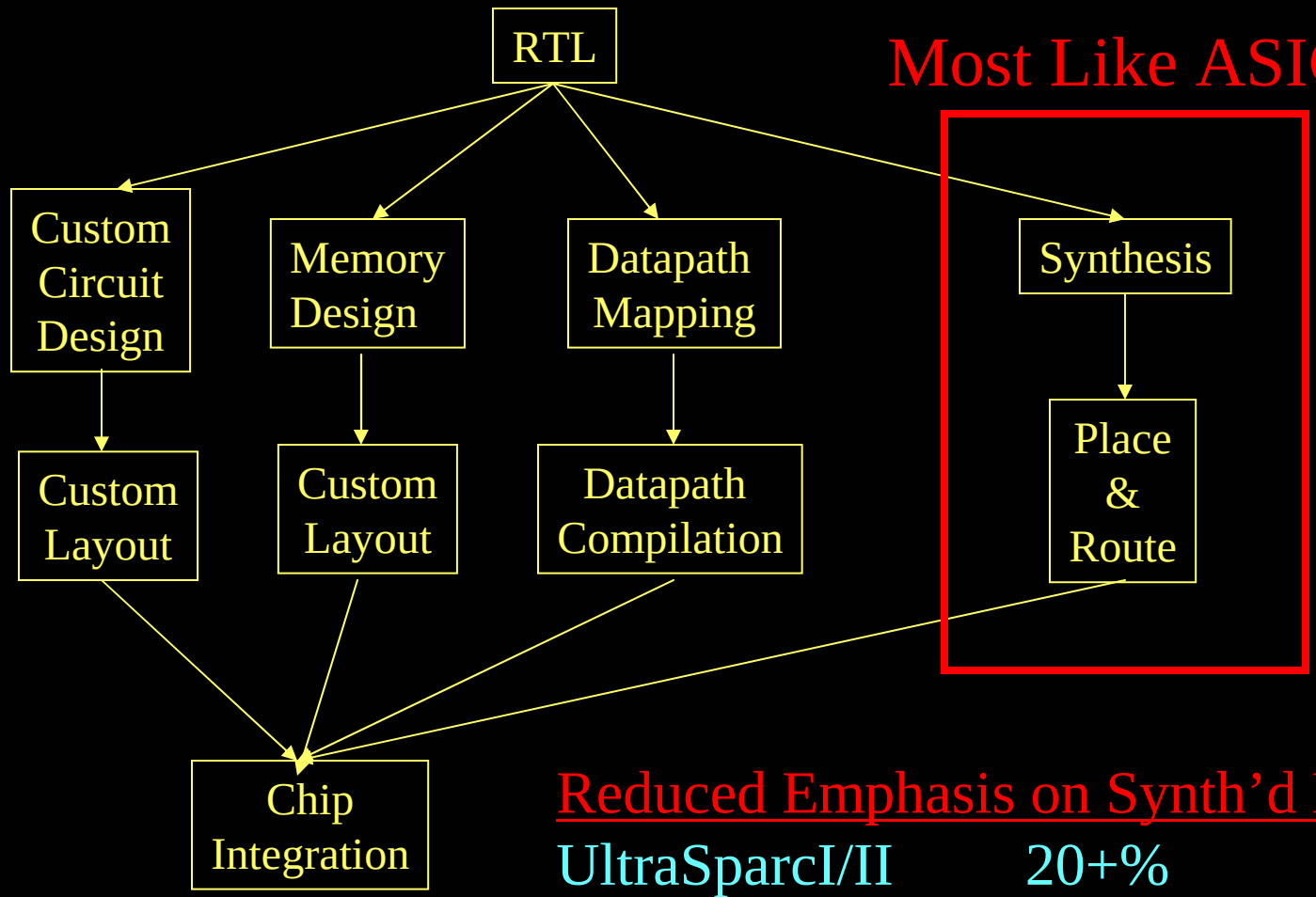
Physical design determines target within a process distribution.

- Clock
- Power
- Signal Integrity
- Performance Verification

Yield and Performance

- ASICs target full yield at target performance.
  - Clock rate often defined by system interface
  - No value in running faster.
  - Non-functional if slower.
- Processors typically do not target full yield at target performance.
  - Marketable at many performance points.
  - Added value for higher performance parts, even if yield is limited.
  - Can still sell slower parts.

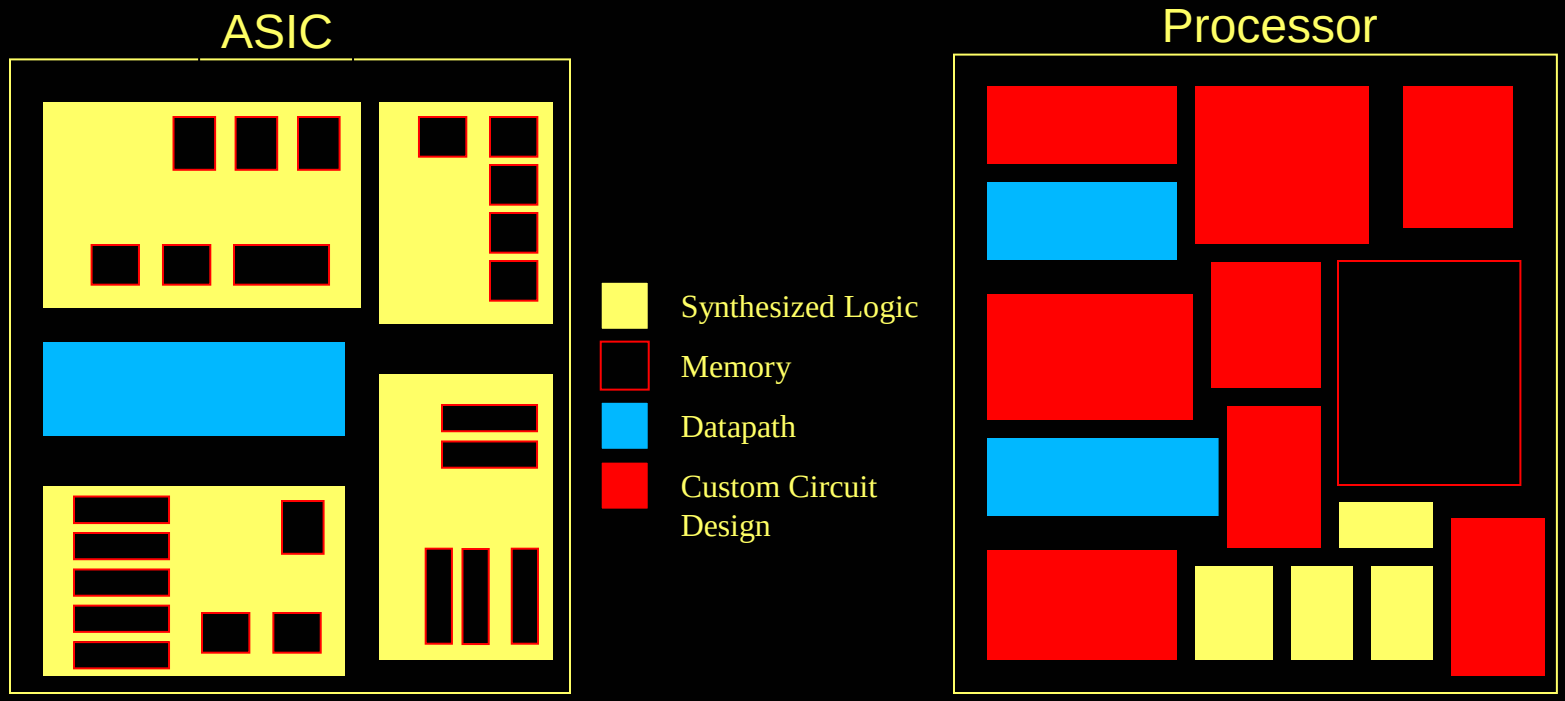
Microprocessor Design Flow Overview



Reduced Emphasis on Synth'd Logic

UltraSparcI/II	20+%
UltrasparcIII	15%
Next Gen Sparc	5%

Key Differences in Design Content



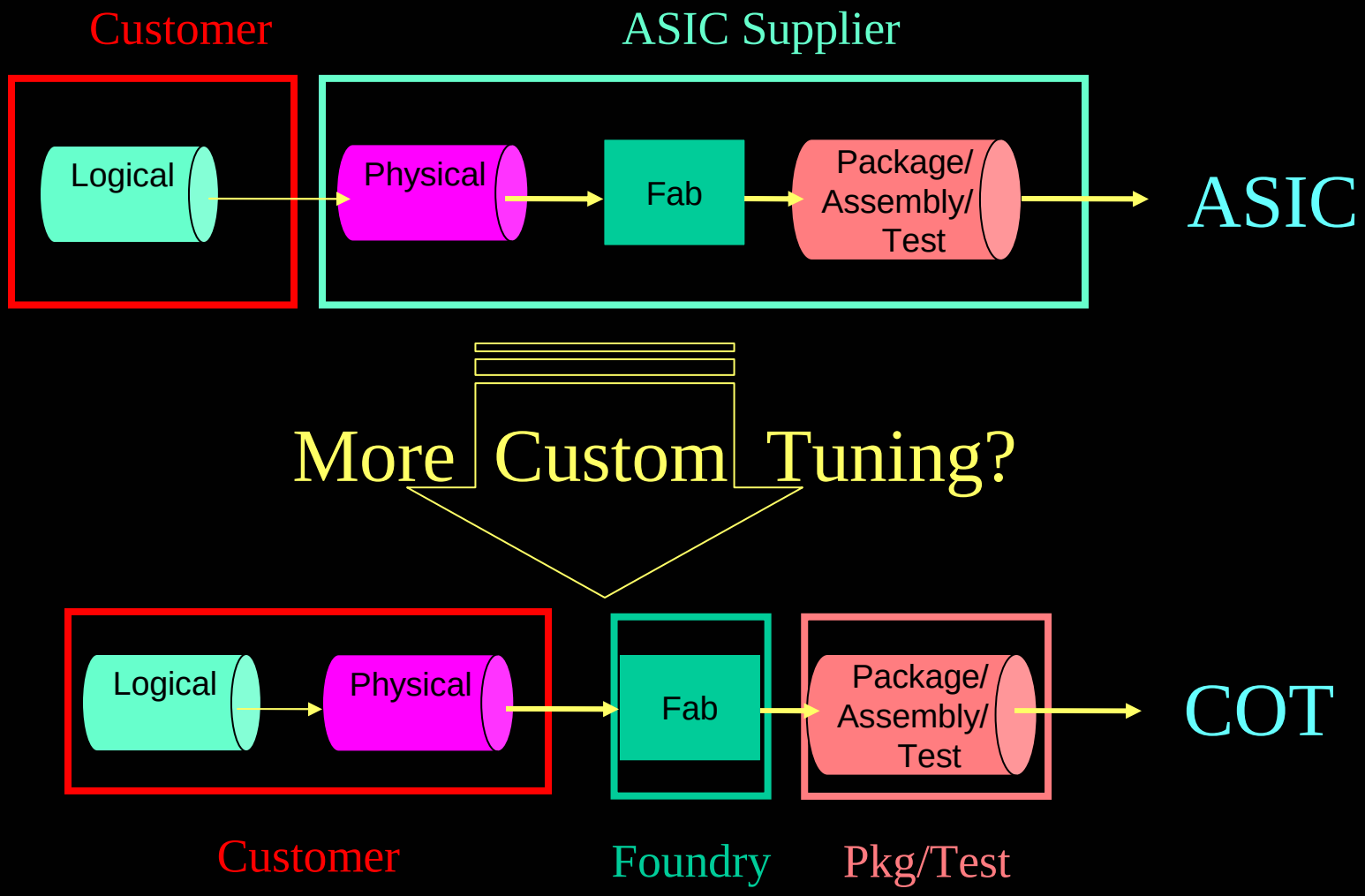
- Dominated by synthesized logic
- Compiled memories embedded in logic.
- Lightly partitioned.

- Dominated by custom circuit design.
- Custom memories as independent blocks.
- Heavily partitioned.

Key Methodology Differences

	ASIC	Processor
Block Size	100's of K gates	10's of K gates
Timing Sign-off	Delay Calculation	Circuit Simulation
Timing Closure	Automated	Manual
Power & Clock	Synthesized	Custom
Noise Analysis	Modeled	Simulated
Noise Repair	Automated	Manual

Migrating to COT



Not Necessarily. . .

If Customer Owns Physical Design, Why Not Tune It?

- ASIC content is fundamentally different than processor content.
- Volatile system IP is partitioned onto ASICs
  - Highly tuned system interfaces
  - Definition evolves right up to system power-on.
- Rapid silicon implementation is often more important than detailed tuning.
- Even if customer owns physical design, the nature of the system IP may prohibit design tuning.
- Then why go COT? $ $ $ $ $ $ $ $ $ $

Different Design Objectives

- Processor
  - More stable architecture (through partitioning)
  - Achieve best possible timing on limited number of well-understood critical paths.
- System chips
  - Less stable architecture (because of system partitioning)
  - Achieve acceptable timing on large number of unknown critical paths.

Implications

- Processors becoming increasingly unsuitable as proving grounds for prevalent silicon design techniques.
- Excellent vehicles for circuit design and performance-related problems.
- Not representative of system chips
  - Small, homogeneous synthesized logic blocks
  - Heavily partitioned and tuned

Conclusion

- Customer-Owned Tooling is a business model, not a design style.
- Ownership of physical design does not equate to higher performance.
- Performance of system chips is often defined by IP and schedule, not design techniques.
- Heavy partitioning and custom circuit design make processor design increasingly less representative of system chip automation.