

# ISPD Panel: Trends in ASIC Design Flow

#### From a Tool Vendor Perspective

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# **Outline: High End ASIC Design**

- Reference point: "typical" design
- Use of hierarchy in design
- Handoff from logic design to physical design
- Physical tie-ins to synthesis
- Noise problems



# **Typical Q1 2001 ASIC Chip**

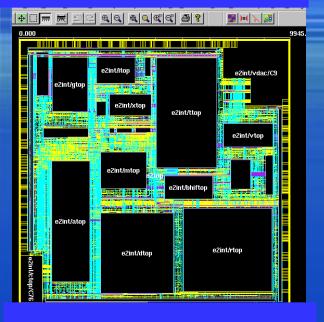
#### **Borderline "SOC"**

- Video Graphic Chip
- Network interface/router chip
- 0.18 u technology, 6 8 layers
- Design
  - 5 large blocks, each with
    - ~12 RAMS
    - 5K pins
    - 250K instances
    - 5 global clocks, 200 derived/gated clocks
    - 27K lines of timing constraints
      - set\_output\_delay 4000 -clock Clk1 -rise -min -add\_delay [get\_ports {MemWriteBus[3]}
      - set\_false\_path -setup -rise -from [get\_pins {GR\_FE\_STAGE1\_CNTRL\_MISC24BIT\_REG\_1\_16A/CK}]

#### • Care abouts

- Correctness
- Timing convergence
- On time delivery

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### **ASIC Flow: Got Hierarchy?**

- All chips have hard blocks in them
- Percent of design starts that are hierarchical increases yearly
  - methodology: insulates sub-projects
  - tool reasons: capacity
  - IP reasons: may not have control over some blocks

 In 2001, about 50% of high-end ASIC chips are "hierarchical" and have soft blocks that are placed independently



#### Logic to Physical Flow (simplified)

**Design Planner** 

RTL

Synthesis/Place

Chip Assembly

#### **Chip Finishing**

GDSII

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**Chip RTL Planning** Synthesis1, Floorplan Generation, Chip Level Time Budgeting

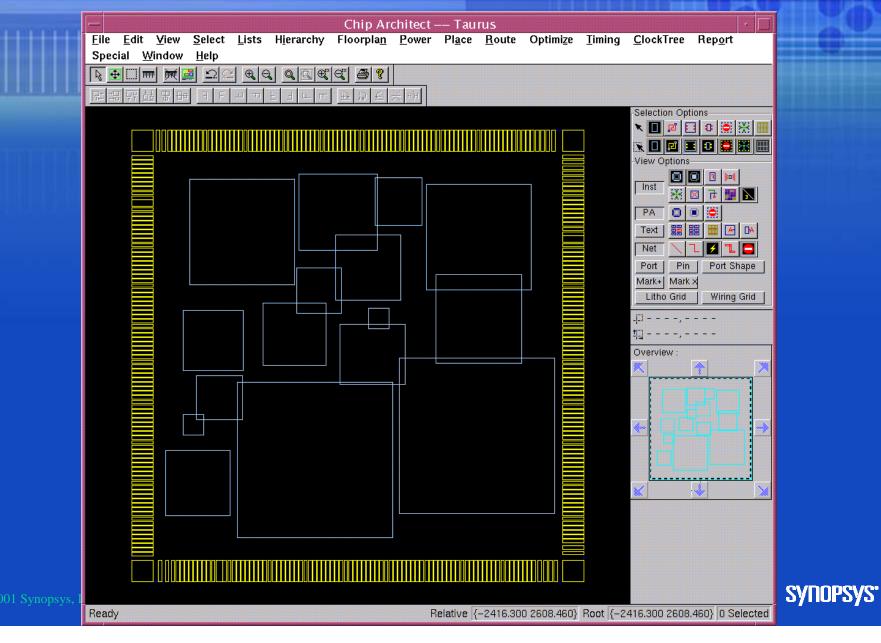
**Block Implementation** 

Synthesis2 & Placement Block routing

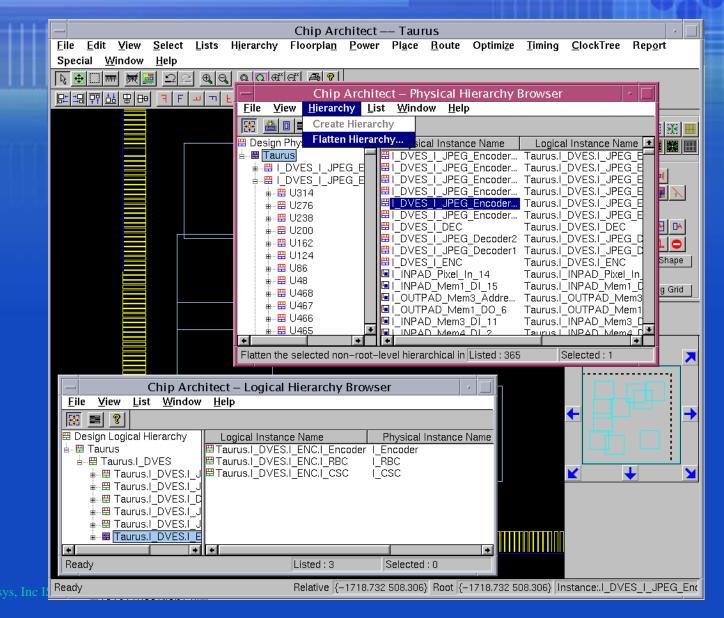
Chip Integration Chip Timing Closure: Pins, Buffers, Global Routing

Finalize Top Level Routing, Extraction, Address (or ignore) Signal Integrity Issues, LVS+DRC

## **Black Box from Initial RTL model**

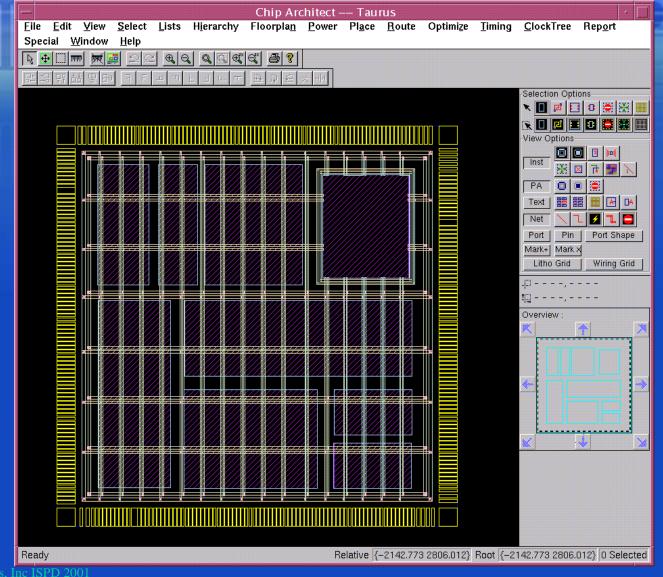


### **Tying Logical to Physical Blocks**



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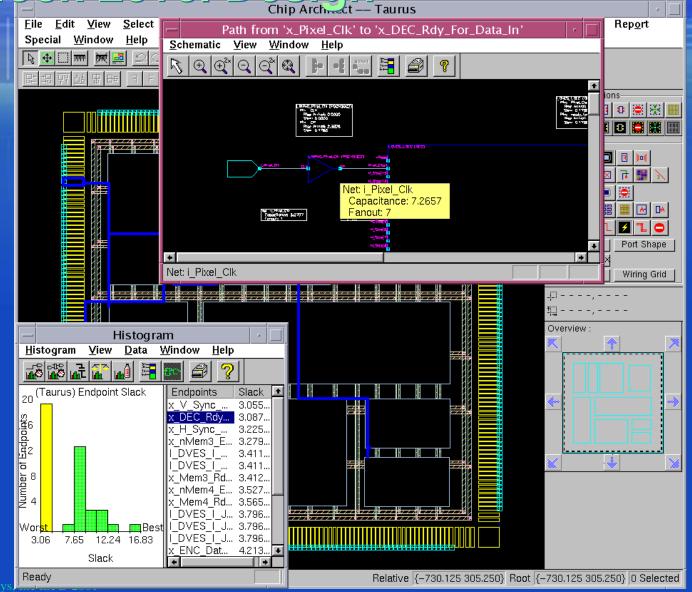
# **Getting More Physical**



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### Realistic Timing Numbers after Block Level Design

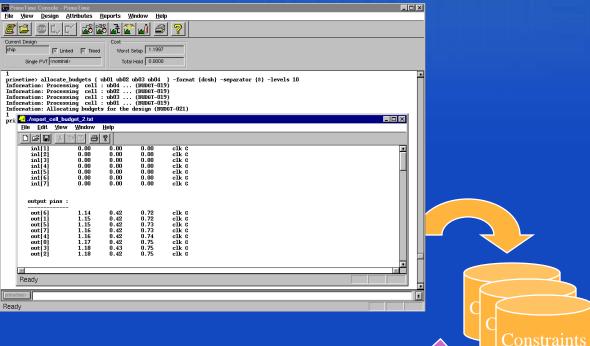


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#### **Key to Timing Closure: Time** Budgeting • Applied at many levels: chip, block, path... File View Design Attributes Reports Window Heli Current Design 🖂 Linked 🕅 Timed Single PVT <nominal> Total Hold 0.0000

Start after entities are identified, not necessarily defined



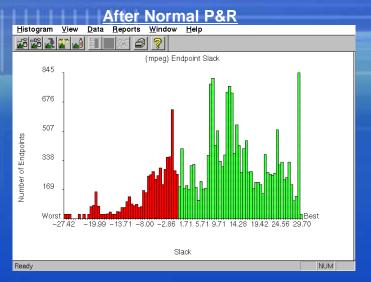
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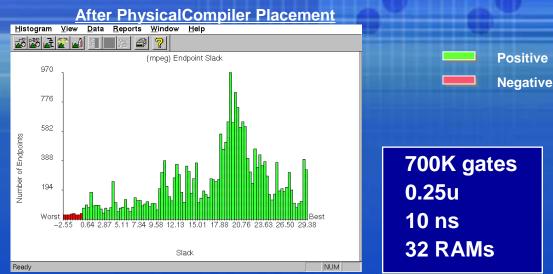
# Block Implementation: Core of Physical Synthesis

- Physical Synthesis
  - turn generic logic gates with no placement into
  - optimized gates with detailed placement
- Requires context from chip:
  - shape
  - obstructions
  - pin positions
  - timing constraints, etc



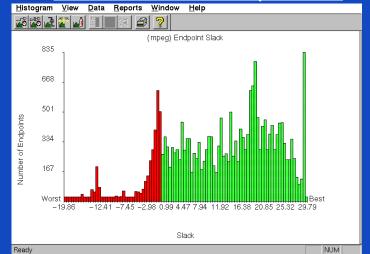
# **Timing Effect of Physical Synthesis**



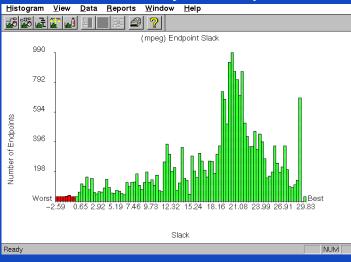


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#### After Normal P&R + Post Optimization



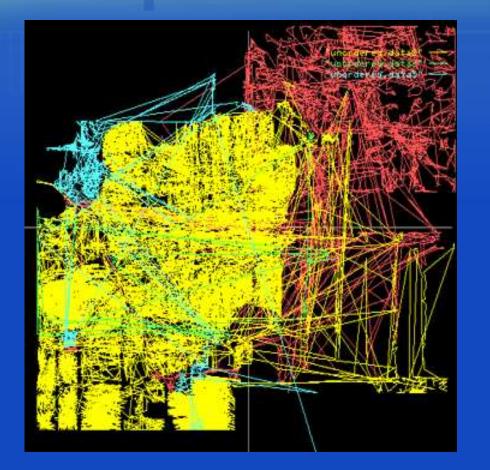
#### After Wroute with PhysicalCompiler Placement

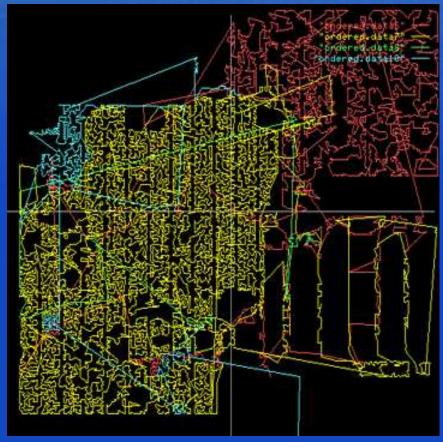


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# Integration of Physical Synthesis: Linking with Test

Path reordering can be chosen to reduce wiring congestion





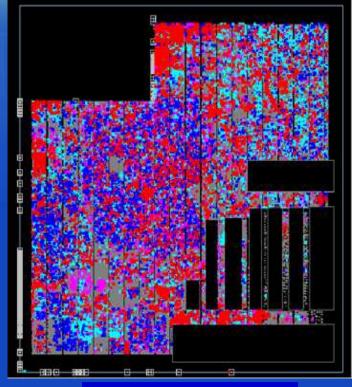
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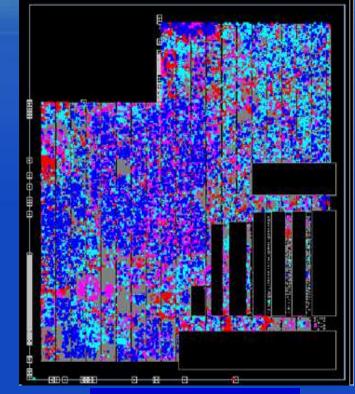
#### Physical Synthesis & Power Analysis Physical Compiler --- Encoder1\_dct\_guantizer <u>File Edit View Select Help</u> R Q Q R K K B ? 📕 🕪 🛅 🏂 SNAPSHOT Selection to Bucket Leafs to Bucket Clear Buckets Visibility 💌 Select - Pref. Cell Ψ ... Port Port $\mathbf{\nabla}$ ... Port Shape ... E Pin $\overline{\mathbf{M}}$ ... 🔽 Net -... C Obstruction ... Place Area 💌 ... Wire Keepout ... PA Keepout ... 🔽 Text -... \_\_\_\_\_ 10 - - - -, - - - -🔽 S0 🔽 S1 □ S2 □ S3 □ S7 -🗆 S4 🗆 S5 S6 SNAPSHOT ..... <u>U</u>pdate Gray Ready Relative {228.84 - 74.26} Root {228.84 - 74.26} 0 Selected psyn\_gui-t> set\_switching\_activity -clock x\_Pixel\_Clk -toggle\_rate 0.5 -static\_prob 0.015 [get\_pin -hierarchical \*] prom\_gui\_t> act guitching\_activity \_clock x\_Pixel\_Clk \_toggle\_rate 0.2 \_static\_prob 0.015 [get\_pin -hierarchical \*] psyn\_gui-t> set\_switching\_activity -clock x\_Pixel\_Clk -toggle\_rate 0.3 -static\_prob 0.015 [get\_net -hierarchical \* ] psyn\_gui-t> set\_switching\_activity -clock x\_Pixel\_Clk -toggle\_rate 0.3 -static\_prob 0.015 [ get\_net -hierarchical \* ] psyn\_gui-t> report\_power -nosplit -cell -sort\_mode cell\_internal\_power ٠ ▶ psyn\_gui-t> SYNOPSYS<sup>•</sup> © 2001 Synopsys, In **Command Line** $\bigwedge$ History $\lambda$ Errors & Warnings $\lambda$ Report /

### Phy. Synthesis & Power Optimization

Gates can be resynthesized based on wire length
Gated clocks can be inserted by proximity



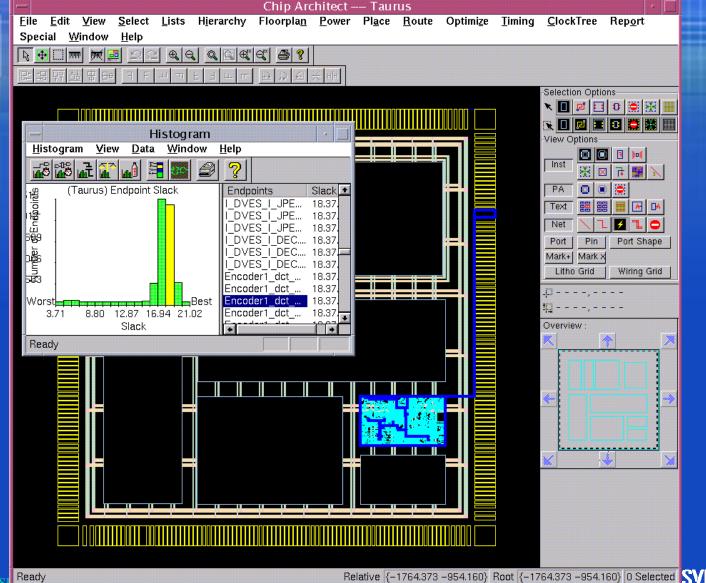
**Power Consumed = 2.4W** 



**Power Consumed = 1.2W** 

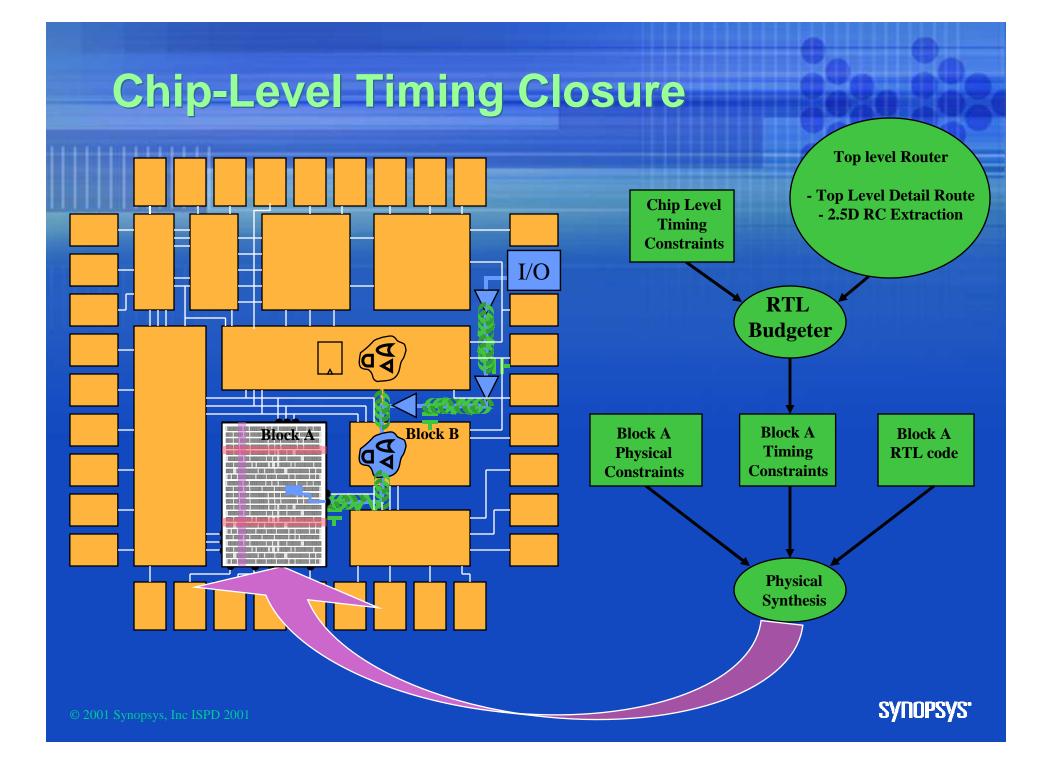
SYNOPSYS<sup>•</sup>

# **Assembly of Blocks into chip**



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Relative {-1764.373 -954.160} Root {-1764.373 -954.160} 0 Selected SVN0PSVS\*



Summary: High End ASIC compared to MicroProcessor
Typical High End design - integration of subsystems, each of which has its own specs. Complexity similar to microprocessor.

- Use of hierarchy in design: required
- Handoff from logic design to physical design: no such thing
- Physical tie-ins to synthesis: several, and growing. But automated, not manual
- Noise problems: ominous, ignored at some peril