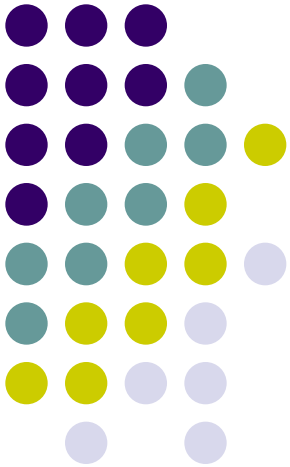
SEMICON Solutions

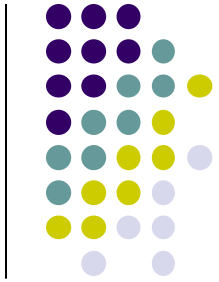
CMOS Logic



Trình bày: Đặng Tường Dương

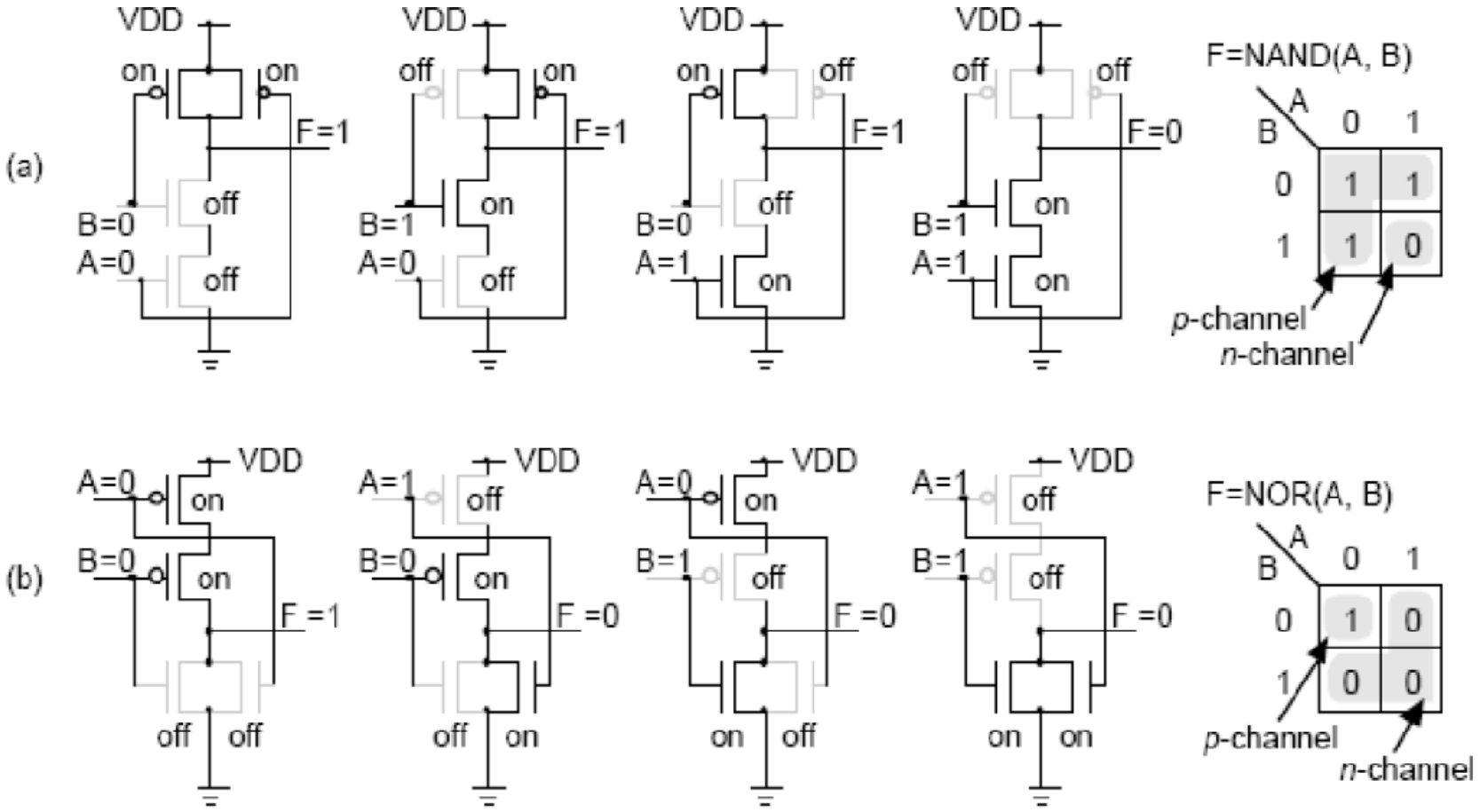
SEMICON
THINKING OUT OF THE BOX

Agenda



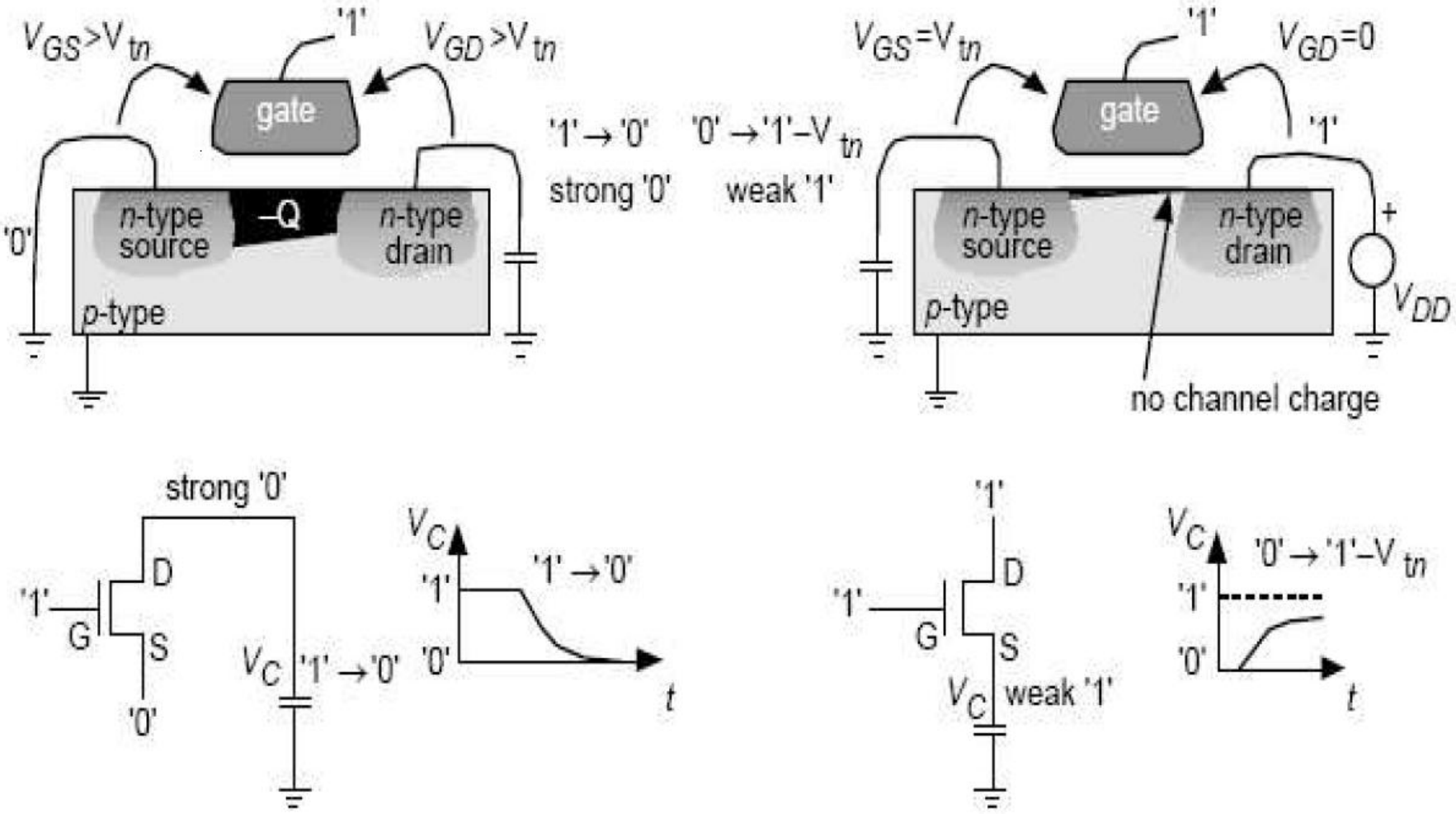
- CMOS logic
- Logic levels
- Transmission Gates
- Sequential Logic Cells
- Datapath Logic Cells

CMOS Logic

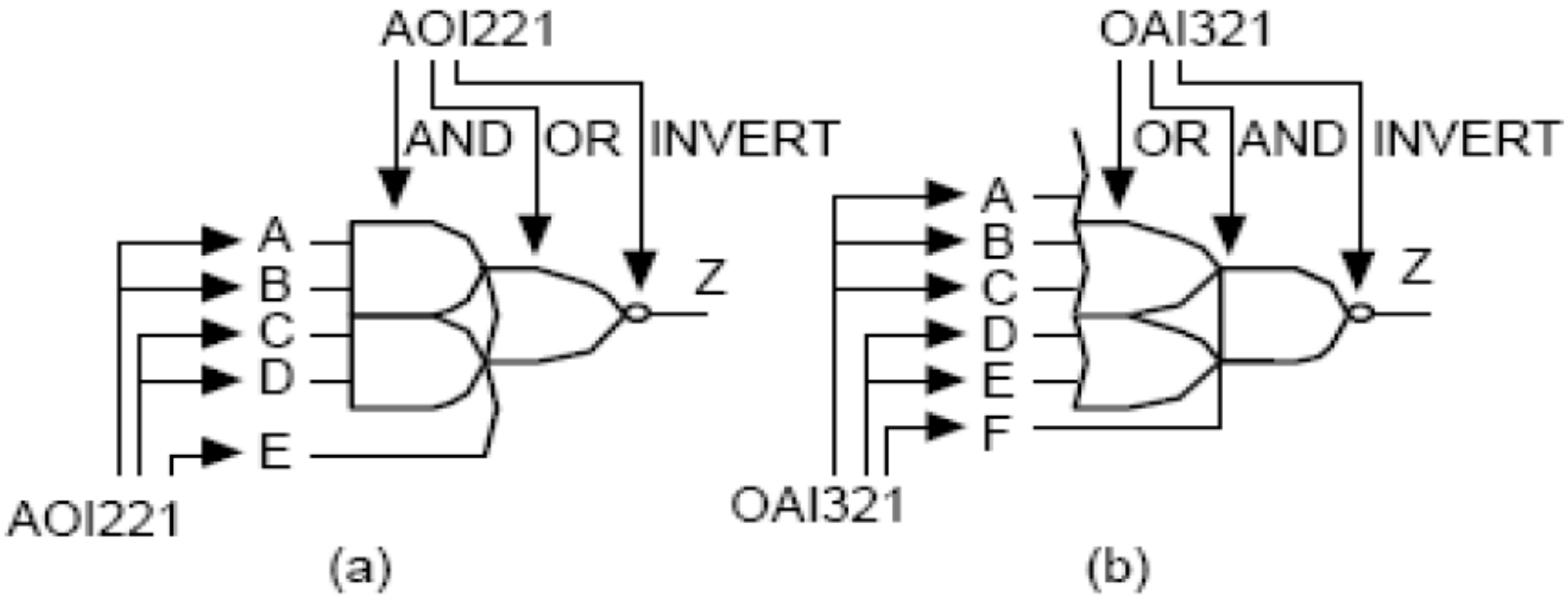


CMOS logic • a two-input **NAND gate** • a two-input **NOR gate** • **Good '1's** • **Good '0's**

Logic Levels



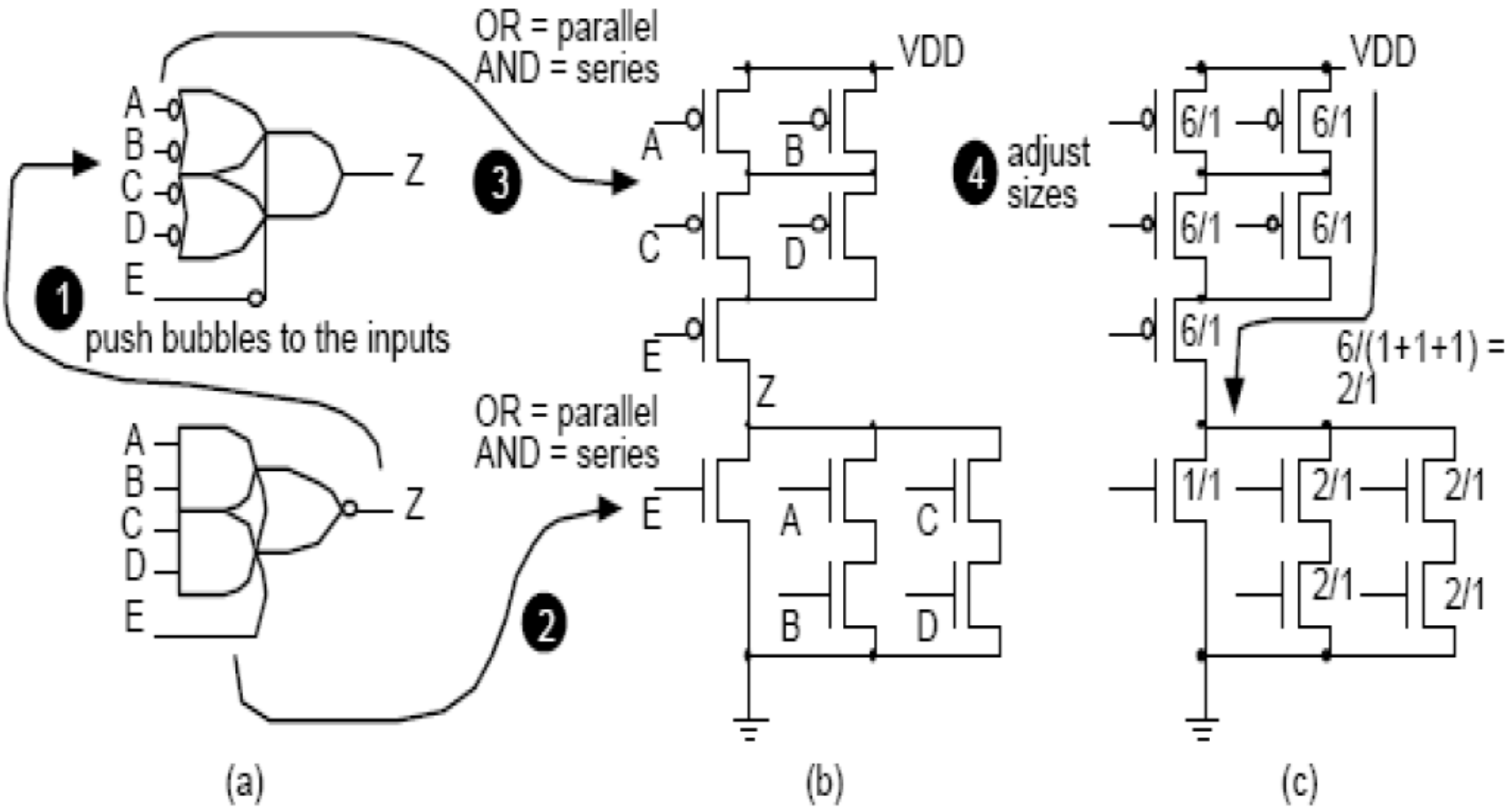
Naming of complex CMOS combinational logic cells



Drive Strength

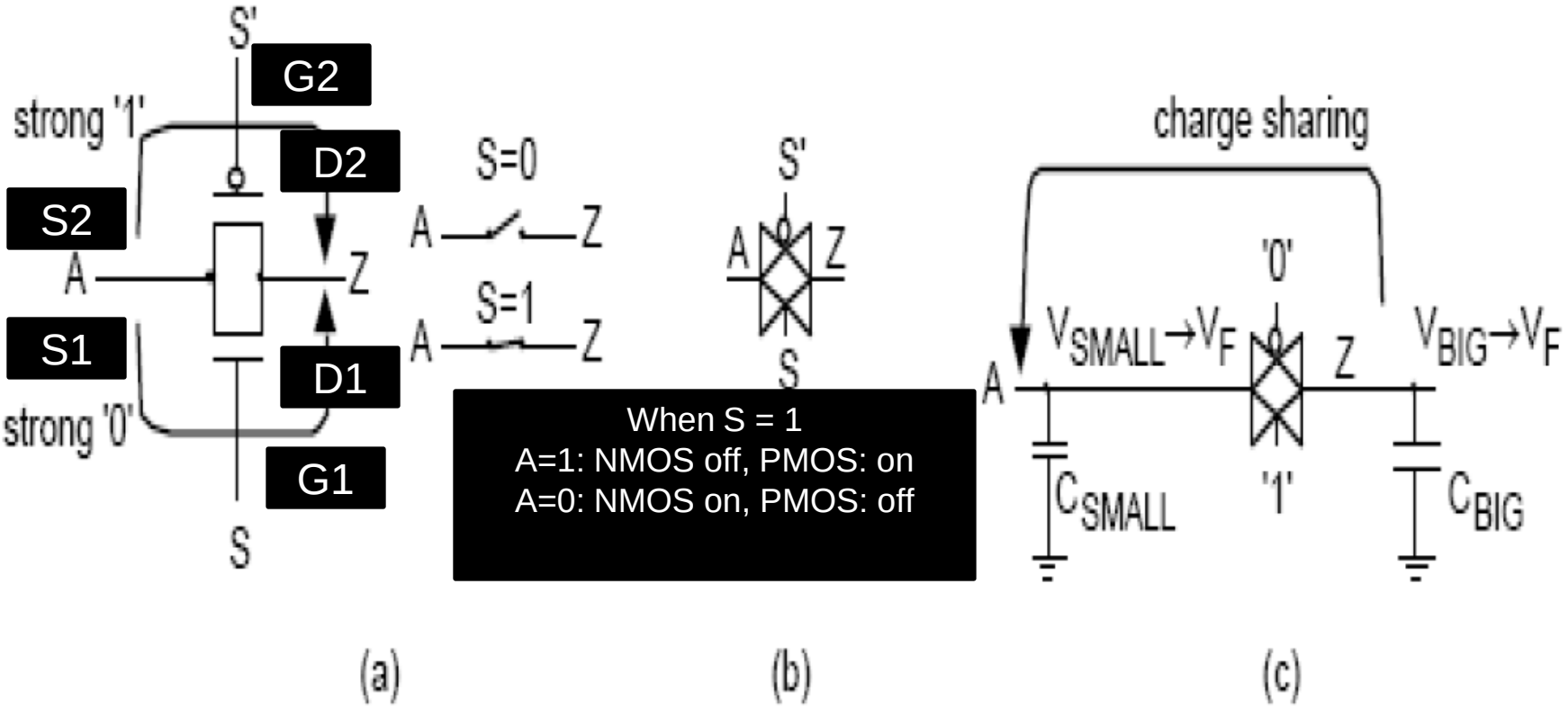
We **ratio** a cell to adjust its **drive strength** and make b*n*=b*p* to create equal rise and fall times

Naming of complex CMOS combinational logic cells

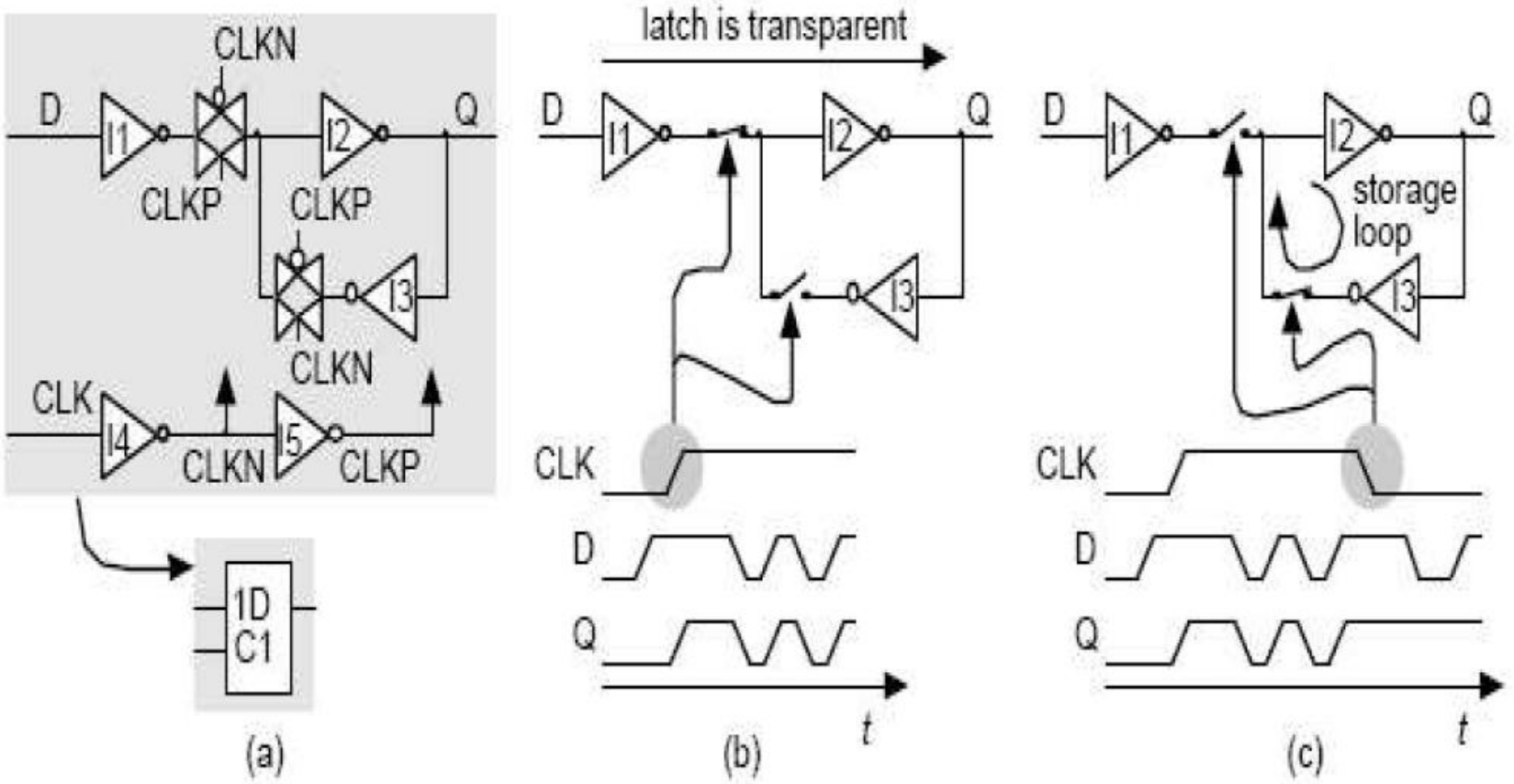


Transmission Gates

CMOS transmission gate (TG, TX gate, pass gate, coupler)

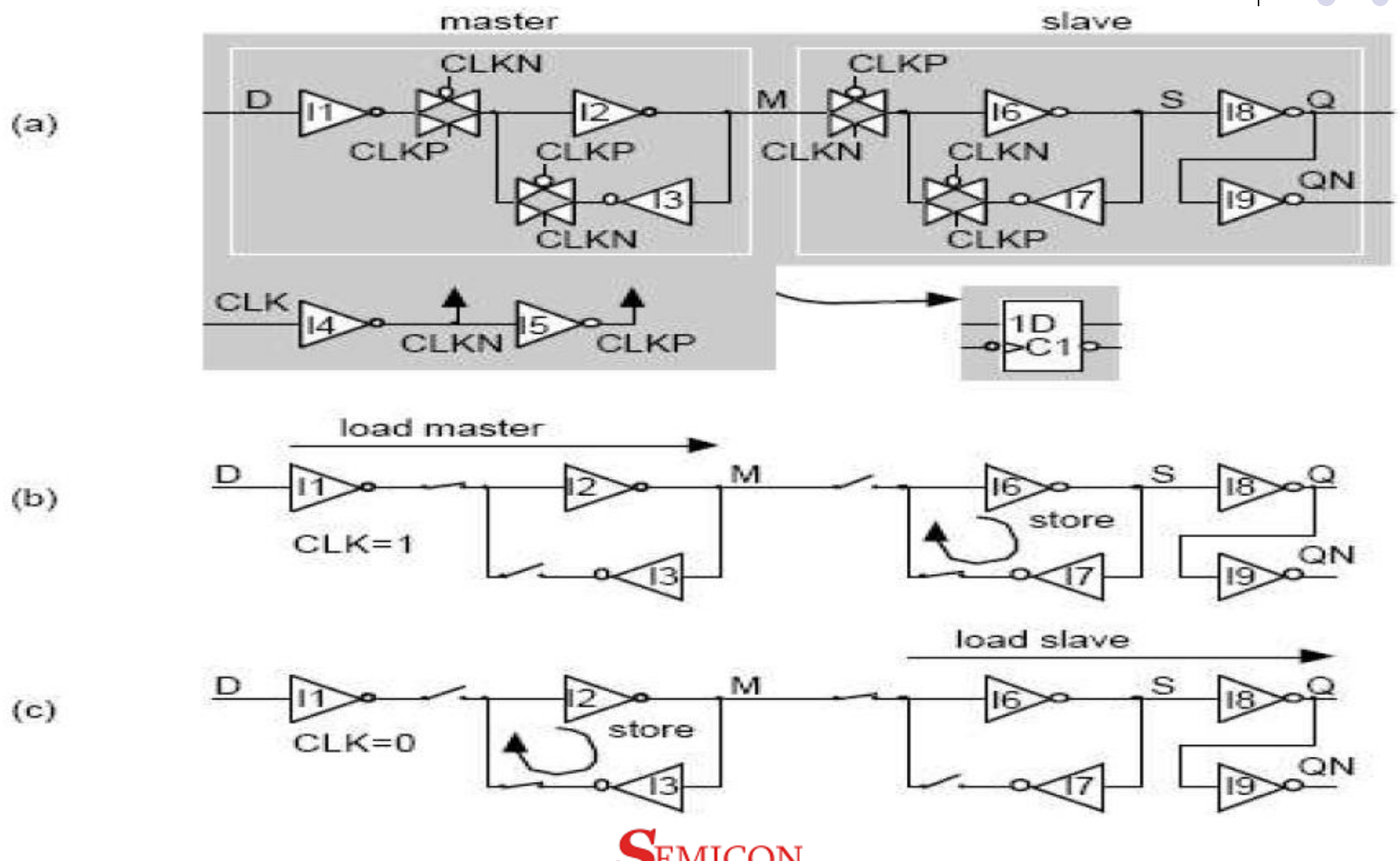


Sequential Logic Cells

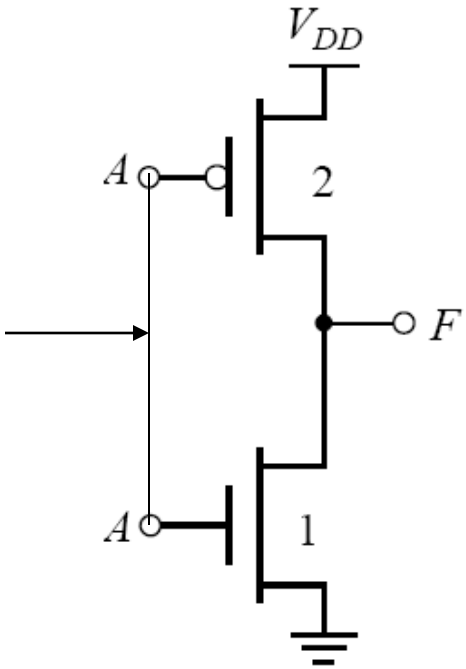


CMOS latch • **enable** • **transparent** • **static** • **sequential logic cell** • **storage** • **initial value**

CMOS flip-flop

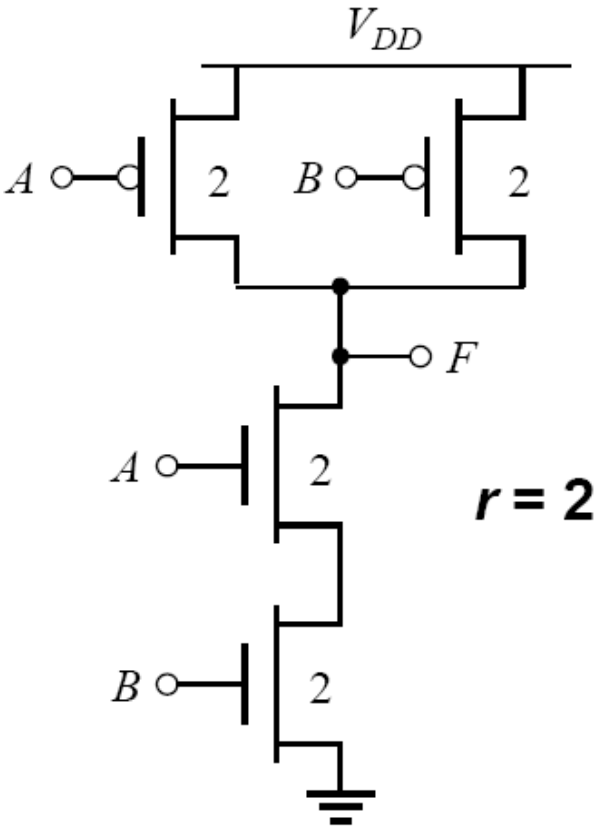


Example of Basic Gates



Inverter

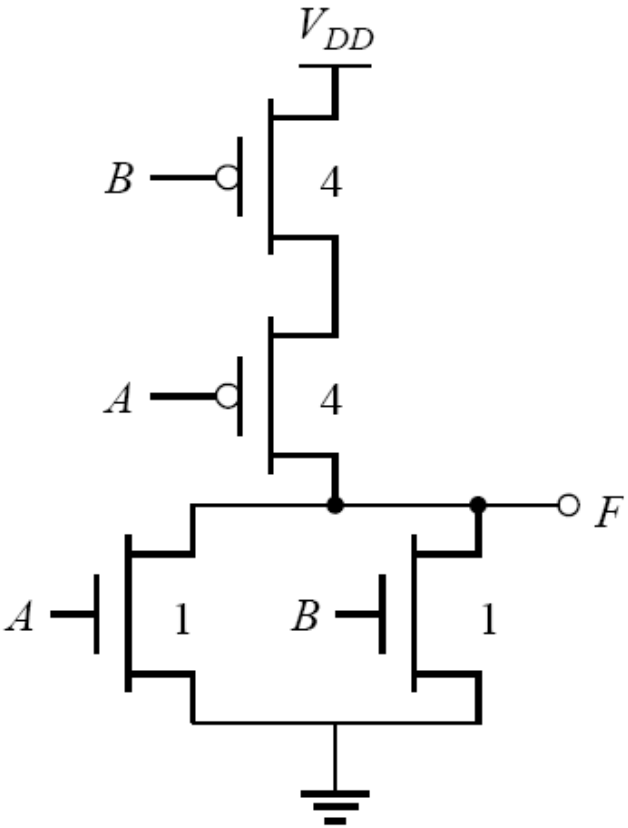
g = 1



2-input NAND

r = 2

g = 4/3



2-input NOR

g = 5/3

Câu Hỏi & Trả Lời