EE260 Introduction to Digital Design

Lecture 6b: Timing Hazards

Behavior of Digital Circuits: Steady State vs. Transient

- We have been analyzing and designing digital circuits assuming **steady-state** conditions:
  - The circuit is stable: the inputs have been applied a long time ago and they have never changed since, so that all gates have had enough time to compute their outputs
  - Alternatively, we can think of it as if all the gates are ideally fast – they react immediately to the changes at the input.
- In reality, **transient** behavior is important:
  - Each gate has a finite (not 0) delay from the time inputs change to the time the change effects their outputs.
- Transient behavior has two main consequences:
  - Circuits have overall finite **delays** (important for performance evaluation)
  - Circuits might have **glitches** at their outputs

Glitches and Hazards

- *Glitch*: pulse due to finite propagation time, when steady state analysis predicts no change in the signal
- *Hazard*: Exists when a circuit has the possibility of a glitch
  - Depends on exact delays or other electrical features of the components
- Key Point: in certain cases, we need to avoid all glitches. To be sure, we need to eliminate all hazards
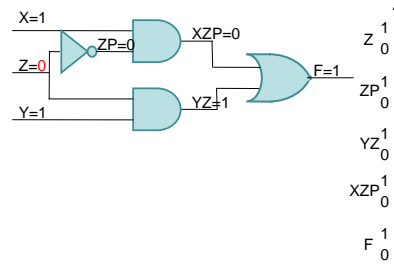
Glitch Example
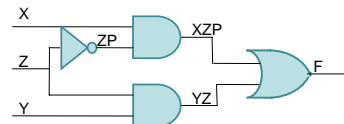
Glitch Example

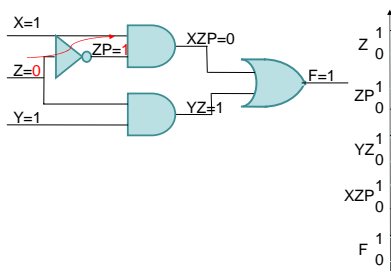- Suppose that, initially, X=Y=Z=1 – and the circuit is stable

X=1
ZP=0
Z=1
XZP=0
Y=1
YZ=1
F=1
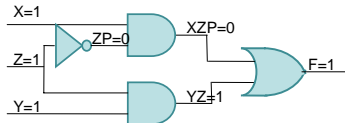
Glitch Example

- Then, input Z changes from 1 to 0: for a while the other signals maintain their values

X=1
ZP=0
Z=0
XZP=0
Y=1
YZ=1
F=1

Z, ZP, YZ, XZP, F

Glitch Example

- After the delay of the inverter ZP changes responding to the new input

X=1
ZP=1
Z=0
XZP=0
Y=1
YZ=1
F=1

Z, ZP, YZ, XZP, F

Glitch Example

- After the delay of the second AND, YZ changes responding to the new input
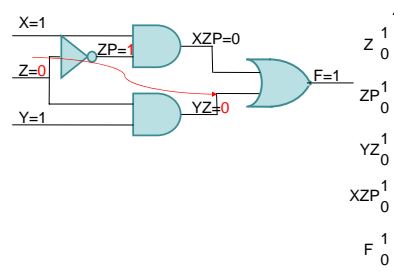
X=1
ZP=1
Z=0
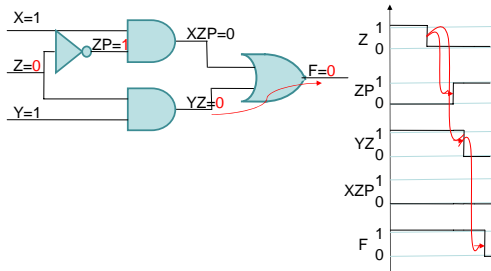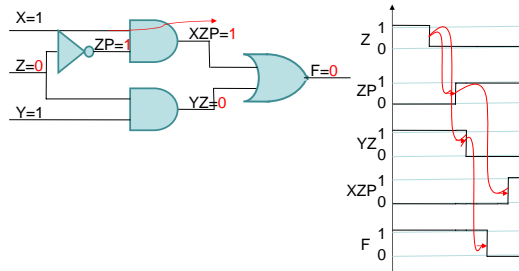XZP=0
Y=1
YZ=0
F=1

Z, ZP, YZ, XZP, F

Glitch Example

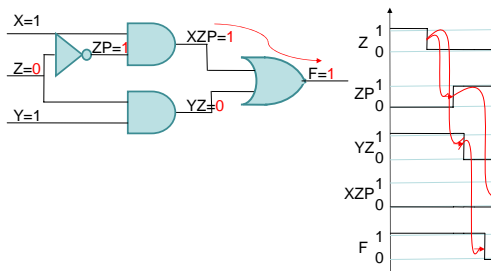- After the delay of the OR, F changes responding to the new YZ

Glitch Example

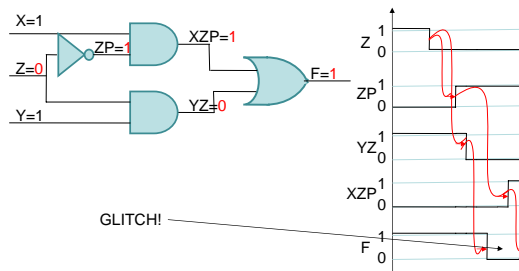- After the delay of the first AND, XZP changes responding to the new ZP

Glitch Example

- Finally, also the latest arrving change of XZP has effect on F

Glitch Example

- Finally, also the latest arrving change of XZP has effect on F

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Static 1-Hazard

- Definition:
  - A circuit has a static 1-Hazard if there exists a pair of input combinations such that:
    - They differ in only 1 input variable
    - Both give an "1" output
    - It is possible for a momentary "0" to occur at the output during a transition between the two inputs
- The previous circuit is an example of static 1-hazard

Static 0-Hazard

- Definition (dual):
  - A circuit has a static 0-Hazard if there exists a pair of input combinations such that:
    - They differ in only 1 input variable
    - Both give an "0" output
    - It is possible for a momentary "1" to occur at the output during a transition between the two inputs
- For example, the dual of the previous circuit is an example of static 0-hazard (see book for other examples)

How do we find hazards?

- If we have a 2-level implementation, analysis can be done on the K-Map!
- It can be proven that:
  - A properly designed AND-OR circuit does not have 0-hazards
  - It has 1-hazards only if there are 2 adjacent 1-cells in the K-Map that are not covered by a single implicant

Finding Hazards - Example

- Previous circuit's K-Map:
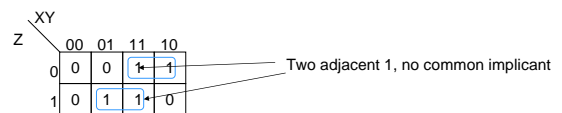
- The <u>reason</u> why there is a hazard is that, when the input Z makes a transition from 0 to 1, two different parts of the circuit are working to guarantee that the output remains 1. If there is delay mismatch, a glitch occurs

Correcting Hazards

- Due to the previous property, we can eliminate 1-hazards by making sure that no adjacent pair of 1 exists that do not belong to the same cube
- Therefore, it is sufficient to find such pairs and add corresponding prime implicants
- We can eliminate hazards by making the circuit more complex – only when needed!

Correcting Hazards - Example

Z \ XY	00	01	11	10
0	0	0	1	1
1	0	1	1	0

Added one implicant – no more hazard

- NOW, when the input Z makes a transition from 0 to 1, one additional portion of the circuit maintains the output at 1, no matter the delays of other parts.

OR-AND and 0-Hazards

- By duality, it is clear that:
  - OR-AND circuits do not have 1-Hazards
  - OR-AND circuits have 0-Hazards if and only if there are two adjacent 0-cells not covered by a single implicant
  - Adding such implicants will eliminate all static hazards

Are there other hazards?

- Dynamic hazards:
  - Consists in an output that is changing more than twice during a single input transition
  - They cannot occur with 2-level circuits
  - They might occur in multi-level circuit
  - See book for examples

Last word about Hazards

- As we will see in the second part of the semester, the traditional (synchronous) design flow allows combinational circuits to have hazards

- Only when designing specialized circuits (asynchronous, or certain elementary components) it is necessary to make sure that hazards do not show up.