# 8-Bit Timers (TMR)

This LSI has two units (unit 0 and unit 1) of an on-chip 8-bit timer module that comprise two 8-bit counter channels, totaling four channels. The 8-bit timer module can be used to count external events and also be used as a multifunction timer in a variety of applications, such as generation of counter reset, interrupt requests, and pulse output with a desired duty cycle using a compare-match signal with two registers.

Figures 11.1 and 11.2 show block diagrams of the 8-bit timer module (unit 0 and unit 1).

This section describes unit 0 (channels 0 and 1), which has the same functions as the other unit.

## 11.1 Features

Selection of seven clock sources

The counters can be driven by one of six internal clock signals (P$\phi$/2, P$\phi$/18, P$\phi$/32, P$\phi$/164, P$\phi$/1024, or P$\phi$/8192) or an external clock input.

Selection of three ways to clear the counters

The counters can be cleared on compare match A or B, or by an external reset signal.

Timer output control by a combination of two compare match signals

The timer output signal in each channel is controlled by a combination of two independent compare match signals, enabling the timer to output pulses with a desired duty cycle or PWM output.

Cascading of two channels (TMR_0 and TMR_1)

Operation as a 16-bit timer is possible, using TMR_0 for the upper 8 bits and TMR_1 for the lower 8 bits (16-bit count mode).

TMR_1 can be used to count TMR_0 compare matches (compare match count mode).

Three interrupt sources

Compare match A, compare match B, and overflow interrupts can be requested independently.

Generation of trigger to start A/D converter conversion

Module stop state specifiable

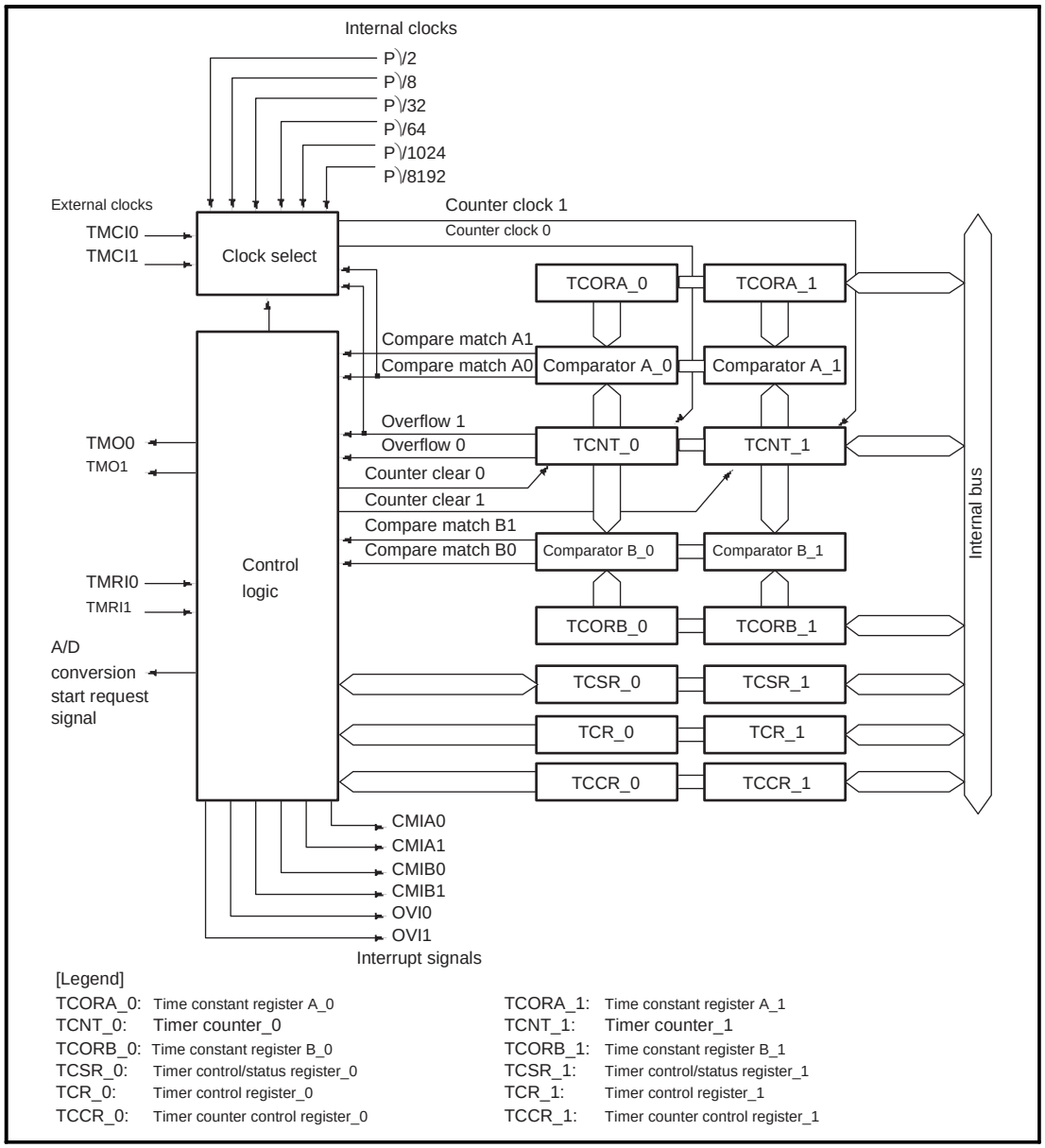



**Figure 11.1 Block Diagram of 8-Bit Timer Module (Unit 0)**

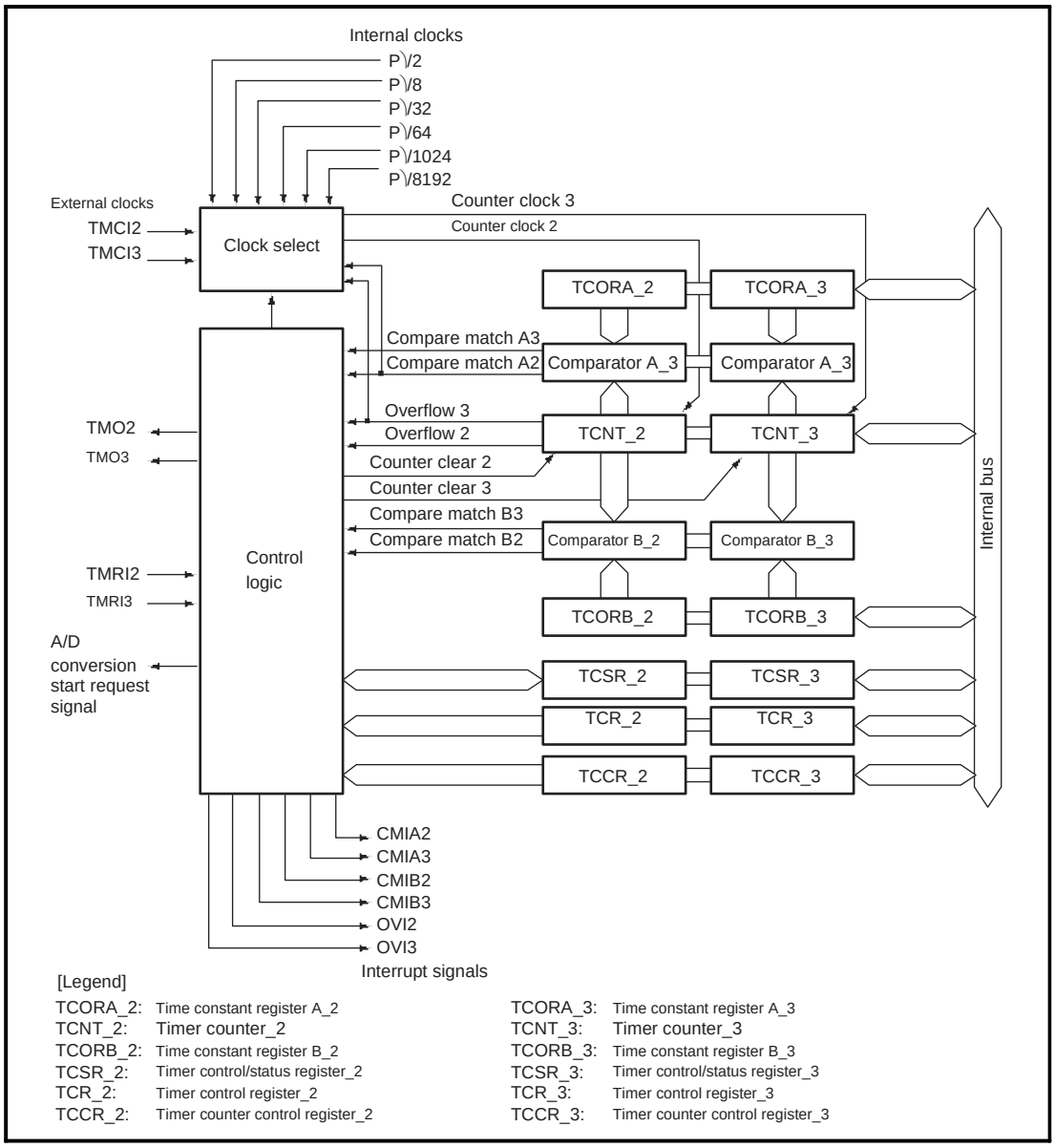



**Figure 11.2 Block Diagram of 8-Bit Timer Module (Unit 1)**

## 11.2 Input/Output Pins

Table 11.1 shows the pin configuration of the TMR.

**Table 11.1 Pin Configuration**

| Unit | Channel | Name | Symbol | I/O | Function |
|---|---|---|---|---|---|
| 0 | 0 | Timer output pin | TMO0 | Output | Outputs compare match |
| | | Timer clock input pin | TMCI0 | Input | Inputs external clock for counter |
| | | Timer reset input pin | TMRI0 | Input | Inputs external reset to counter |
| | 1 | Timer output pin | TMO1 | Output | Outputs compare match |
| | | Timer clock input pin | TMCI1 | Input | Inputs external clock for counter |
| | | Timer reset input pin | TMRI1 | Input | Inputs external reset to counter |
| 1 | 2 | Timer output pin | TMO2 | Output | Outputs compare match |
| | | Timer clock input pin | TMCI2 | Input | Inputs external clock for counter |
| | | Timer reset input pin | TMRI2 | Input | Inputs external reset to counter |
| | 3 | Timer output pin | TMO3 | Output | Outputs compare match |
| | | Timer clock input pin | TMCI3 | Input | Inputs external clock for counter |
| | | Timer reset input pin | TMRI3 | Input | Inputs external reset to counter |

## 11.3 Register Descriptions

The TMR has the following registers.

**Unit 0:**

Channel 0
- Timer counter_0 (TCNT_0)
- Time constant register A_0 (TCORA_0)
- Time constant register B_0 (TCORB_0)
- Timer control register_0 (TCR_0)
- Timer counter control register_0 (TCCR_0)
- Timer control/status register_0 (TCSR_0)

Channel 1
- Timer counter_1 (TCNT_1)
- Time constant register A_1 (TCORA_1)
- Time constant register B_1 (TCORB_1)
- Timer control register_1 (TCR_1)
- Timer counter control register_1 (TCCR_1)
- Timer control/status register_1 (TCSR_1)

**Unit 1:**

Channel 2
- Timer counter_2 (TCNT_2)
- Time constant register A_2 (TCORA_2)
- Time constant register B_2 (TCORB_2)
- Timer control register_2 (TCR_2)
- Timer counter control register_2 (TCCR_2)
- Timer control/status register_2 (TCSR_2)

Channel 3
- Timer counter_3 (TCNT_3)
- Time constant register A_3 (TCORA_3)
- Time constant register B_3 (TCORB_3)
- Timer control register_3 (TCR_3)
- Timer counter control register_3 (TCCR_3)
- Timer control/status register_3 (TCSR_3)

### 11.3.1 Timer Counter (TCNT)

TCNT is an 8-bit readable/writable up-counter. TCNT_0 and TCNT_1 comprise a single 16-bit register so they can be accessed together by a word transfer instruction. Bits CKS2 to CKS0 in TCR and bits ICKS1 and ICKS0 in TCCR are used to select a clock. TCNT can be cleared by an external reset input signal, compare match A signal, or compare match B signal. Which signal is to be used for clearing is selected by bits CCLR1 and CCLR0 in TCR. When TCNT overflows from H'FF to H'00, bit OVF in TCSR is set to 1. TCNT is initialized to H'00.

| | TCNT_0 | | | | | | | | TCNT_1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit Name | | | | | | | | | | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

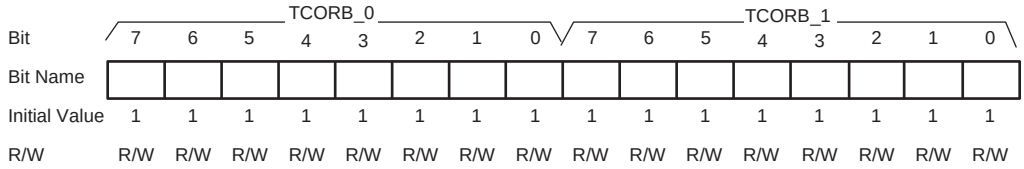
### 11.3.2 Time Constant Register A (TCORA)

TCORA is an 8-bit readable/writable register. TCORA_0 and TCORA_1 comprise a single 16-bit register so they can be accessed together by a word transfer instruction. The value in TCORA is continually compared with the value in TCNT. When a match is detected, the corresponding CMFA flag in TCSR is set to 1. Note however that comparison is disabled during the T2 state of a TCORA write cycle. The timer output from the TMO pin can be freely controlled by this compare match signal (compare match A) and the settings of bits OS1 and OS0 in TCSR. TCORA is initialized to H'FF.

| | TCORA_0 | | | | | | | | TCORA_1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit Name | | | | | | | | | | | | | | | | |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

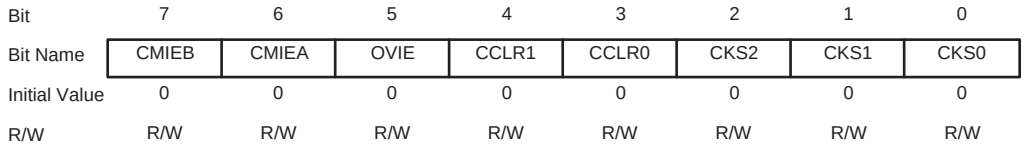
### 11.3.3 Time Constant Register B (TCORB)

TCORB is an 8-bit readable/writable register. TCORB_0 and TCORB_1 comprise a single 16-bit register so they can be accessed together by a word transfer instruction. TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding CMFB flag in TCSR is set to 1. Note however that comparison is disabled during the T2 state of a TCORB write cycle. The timer output from the TMO pin can be freely controlled by this compare match signal (compare match B) and the settings of bits OS3 and OS2 in TCSR. TCORB is initialized to H'FF.




### 11.3.4 Timer Control Register (TCR)

TCR selects the TCNT clock source and the condition for clearing TCNT, and enables/disables interrupt requests.




| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | CMIEB | 0 | R/W | Compare Match Interrupt Enable B<br>Selects whether CMFB interrupt requests (CMIB) are enabled or disabled when the CMFB flag in TCSR is set to 1.<br>0: CMFB interrupt requests (CMIB) are disabled<br>1: CMFB interrupt requests (CMIB) are enabled |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 6 | CMIEA | 0 | R/W | Compare Match Interrupt Enable A<br>Selects whether CMFA interrupt requests (CMIA) are enabled or disabled when the CMFA flag in TCSR is set to 1.<br>0: CMFA interrupt requests (CMIA) are disabled<br>1: CMFA interrupt requests (CMIA) are enabled |
| 5 | OVIE | 0 | R/W | Timer Overflow Interrupt Enable<br>Selects whether OVF interrupt requests (OVI) are enabled or disabled when the OVF flag in TCSR is set to 1.<br>0: OVF interrupt requests (OVI) are disabled<br>1: OVF interrupt requests (OVI) are enabled |
| 4 | CCLR1 | 0 | R/W | Counter Clear 1 and 0* |
| 3 | CCLR0 | 0 | R/W | These bits select the method by which TCNT is cleared.<br>00: Clearing is disabled<br>01: Cleared by compare match A<br>10: Cleared by compare match B<br>11: Cleared at rising edge (TMRIS in TCCR is cleared to 0) of the external reset input or when the external reset input is high (TMRIS in TCCR is set to 1) |
| 2 | CKS2 | 0 | R/W | Clock Select 2 to 0* |
| 1 | CKS1 | 0 | R/W | These bits select the clock input to TCNT and count condition. See table 11.2. |
| 0 | CKS0 | 0 | R/W | |

Note: * To use an external reset or external clock, the DDR and ICR bits in the corresponding pin should be set to 0 and 1, respectively. For details, see section 8, I/O Ports.

### 11.3.5 Timer Counter Control Register (TCCR)

TCCR selects the TCNT internal clock source and controls external reset input.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | | | | | TMRIS | | ICKS1 | ICKS0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 4 | | 0 | R/W | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 3 | TMRIS | 0 | R/W | Timer Reset Input Select<br>Selects an external reset input when the CCLR1 and CCLR0 bits in TCR are B'11.<br>0: Cleared at rising edge of the external reset<br>1: Cleared when the external reset is high |
| 2 | | 0 | R/W | Reserved<br>This bit is always read as 0. The write value should always be 0 |
| 1 | ICKS1 | 0 | R/W | Internal Clock Select 1 and 0 |
| 0 | ICKS0 | 0 | R/W | These bits in combination with bits CKS2 to CKS0 in TCR select the internal clock. See table 11.2. |

**Table 11.2 Clock Input to TCNT and Count Condition**

| | TCR | | | TCCR | | |
|---|---|---|---|---|---|---|
| Channel | Bit 2 CKS2 | Bit 1 CKS1 | Bit 0 CKS0 | Bit 1 ICKS1 | Bit 0 ICKS0 | Description |
| TMR_0 | 0 | 0 | 0 | | | Clock input prohibited. |
| | 0 | 0 | 1 | 0 | 0 | Uses internal clock. Counts at rising edge of P$\phi$/8. |
| | | | | 0 | 1 | Uses internal clock. Counts at rising edge of P$\phi$/2. |
| | | | | 1 | 0 | Uses internal clock. Counts at falling edge of P$\phi$/8. |
| | | | | 1 | 1 | Uses internal clock. Counts at falling edge of P$\phi$/2. |
| | 0 | 1 | 0 | 0 | 0 | Uses internal clock. Counts at rising edge of P$\phi$/64. |
| | | | | 0 | 1 | Uses internal clock. Counts at rising edge of P$\phi$/32. |
| | | | | 1 | 0 | Uses internal clock. Counts at falling edge of P$\phi$/64. |
| | | | | 1 | 1 | Uses internal clock. Counts at falling edge of P$\phi$/32. |
| | 0 | 1 | 1 | 0 | 0 | Uses internal clock. Counts at rising edge of P$\phi$/8192. |
| | | | | 0 | 1 | Uses internal clock. Counts at rising edge of P$\phi$/1024. |
| | | | | 1 | 0 | Uses internal clock. Counts at falling edge of P$\phi$/8192. |
| | | | | 1 | 1 | Uses internal clock. Counts at falling edge of P$\phi$/1024. |
| | 1 | 0 | 0 | | | Counts at TCNT_1 overflow signal*1. |
| TMR_1 | 0 | 0 | 0 | | | Clock input prohibited. |
| | 0 | 0 | 1 | 0 | 0 | Uses internal clock. Counts at rising edge of P$\phi$/8. |
| | | | | 0 | 1 | Uses internal clock. Counts at rising edge of P$\phi$/2. |
| | | | | 1 | 0 | Uses internal clock. Counts at falling edge of P$\phi$/8. |
| | | | | 1 | 1 | Uses internal clock. Counts at falling edge of P$\phi$/2. |
| | 0 | 1 | 0 | 0 | 0 | Uses internal clock. Counts at rising edge of P$\phi$/64. |
| | | | | 0 | 1 | Uses internal clock. Counts at rising edge of P$\phi$/32. |
| | | | | 1 | 0 | Uses internal clock. Counts at falling edge of P$\phi$/64. |
| | | | | 1 | 1 | Uses internal clock. Counts at falling edge of P$\phi$/32. |
| | 0 | 1 | 1 | 0 | 0 | Uses internal clock. Counts at rising edge of P$\phi$/8192. |
| | | | | 0 | 1 | Uses internal clock. Counts at rising edge of P$\phi$/1024. |
| | | | | 1 | 0 | Uses internal clock. Counts at falling edge of P$\phi$/8192. |
| | | | | 1 | 1 | Uses internal clock. Counts at falling edge of P$\phi$/1024. |
| | 1 | 0 | 0 | | | Counts at TCNT_0 compare match A*1. |

| | TCR | | | TCCR | | |
|---|---|---|---|---|---|---|
| Channel | Bit 2 CKS2 | Bit 1 CKS1 | Bit 0 CKS0 | Bit 1 ICKS1 | Bit 0 ICKS0 | Description |
| All | 1 | 0 | 1 | | | Uses external clock. Counts at rising edge*[2]. |
| | 1 | 1 | 0 | | | Uses external clock. Counts at falling edge*[2]. |
| | 1 | 1 | 1 | | | Uses external clock. Counts at both rising and falling edges*[2]. |

Notes: 1. If the clock input of TMR_0 is the TCNT_1 overflow signal and that of TMR_1 is the TCNT_0 compare match signal, no incrementing clock is generated. Do not use this setting.

2. To use the external clock, the DDR and ICR bits in the corresponding pin should be set to 0 and 1, respectively. For details, see section 8, I/O Ports.

### 11.3.6 Timer Control/Status Register (TCSR)

TCSR displays status flags, and controls compare match output.

- TCSR_0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CMFB | CMFA | OVF | ADTE | OS3 | OS2 | OS1 | OS0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/(W)* | R/(W)* | R/(W)* | R/W | R/W | R/W | R/W | R/W |

- TCSR_1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CMFB | CMFA | OVF | | OS3 | OS2 | OS1 | OS0 |
| Initial Value | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| R/W | R/(W)* | R/(W)* | R/(W)* | R | R/W | R/W | R/W | R/W |

Note: * Only 0 can be written to this bit, to clear the flag.

TCSR_0

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | CMFB | 0 | R/(W)*1 | Compare Match Flag B<br>[Setting condition]<br>When TCNT matches TCORB<br>[Clearing conditions]<br>When writing 0 after reading CMFB = 1<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)<br>When the DTC is activated by a CMIB interrupt while the DISEL bit in MRB of the DTC is 0 |
| 6 | CMFA | 0 | R/(W)*1 | Compare Match Flag A<br>[Setting condition]<br>When TCNT matches TCORA<br>[Clearing conditions]<br>When writing 0 after reading CMFA = 1<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)<br>When the DTC is activated by a CMIA interrupt while the DISEL bit in MRB in the DTC is 0 |
| 5 | OVF | 0 | R/(W)*1 | Timer Overflow Flag<br>[Setting condition]<br>When TCNT overflows from H'FF to H'00<br>[Clearing condition]<br>When writing 0 after reading OVF = 1<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.) |
| 4 | ADTE | 0 | R/W | A/D Trigger Enable<br>Selects enabling or disabling of A/D converter start requests by compare match A.<br>0: A/D converter start requests by compare match A are disabled<br>1: A/D converter start requests by compare match A are enabled |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 3 | OS3 | 0 | R/W | Output Select 3 and 2*2 |
| 2 | OS2 | 0 | R/W | These bits select a method of TMO pin output when compare match B of TCORB and TCNT occurs.<br>00: No change when compare match B occurs<br>01: 0 is output when compare match B occurs<br>10: 1 is output when compare match B occurs<br>11: Output is inverted when compare match B occurs (toggle output) |
| 1 | OS1 | 0 | R/W | Output Select 1 and 0*2 |
| 0 | OS0 | 0 | R/W | These bits select a method of TMO pin output when compare match A of TCORA and TCNT occurs.<br>00: No change when compare match A occurs<br>01: 0 is output when compare match A occurs<br>10: 1 is output when compare match A occurs<br>11: Output is inverted when compare match A occurs (toggle output) |

Notes: 1. Only 0 can be written to bits 7 to 5, to clear these flags.
2. Timer output is disabled when bits OS3 to OS0 are all 0. Timer output is 0 until the first compare match occurs after resetting.

TCSR_1

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | CMFB | 0 | R/(W)*1 | Compare Match Flag B<br>[Setting condition]<br>When TCNT matches TCORB<br>[Clearing conditions]<br>When writing 0 after reading CMFB = 1 (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)<br>When the DTC is activated by a CMIB interrupt while the DISEL bit in MRB of the DTC is 0 |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 6 | CMFA | 0 | R/(W)*[1] | Compare Match Flag A<br>[Setting condition]<br>When TCNT matches TCORA<br>[Clearing conditions]<br>When writing 0 after reading CMFA = 1<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)<br>When the DTC is activated by a CMIA interrupt while the DISEL bit in MRB of the DTC is 0 |
| 5 | OVF | 0 | R/(W)*[1] | Timer Overflow Flag<br>[Setting condition]<br>When TCNT overflows from H'FF to H'00<br>[Clearing condition]<br>Cleared by reading OVF when OVF = 1, then writing 0 to OVF<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.) |
| 4 | | 1 | R | Reserved<br>This is a read-only bit and cannot be modified. |
| 3 | OS3 | 0 | R/W | Output Select 3 and 2*[2] |
| 2 | OS2 | 0 | R/W | These bits select a method of TMO pin output when compare match B of TCORB and TCNT occurs.<br>00: No change when compare match B occurs<br>01: 0 is output when compare match B occurs<br>10: 1 is output when compare match B occurs<br>11: Output is inverted when compare match B occurs (toggle output) |
| 1 | OS1 | 0 | R/W | Output Select 1 and 0*[2] |
| 0 | OS0 | 0 | R/W | These bits select a method of TMO pin output when compare match A of TCORA and TCNT occurs.<br>00: No change when compare match A occurs<br>01: 0 is output when compare match A occurs<br>10: 1 is output when compare match A occurs<br>11: Output is inverted when compare match A occurs (toggle output) |

Notes: 1. Only 0 can be written to bits 7 to 5, to clear these flags.

2. Timer output is disabled when bits OS3 to OS0 are all 0. Timer output is 0 until the first compare match occurs after resetting.

## 11.4 Operation

### 11.4.1 Pulse Output

Figure 11.3 shows an example of the 8-bit timer being used to generate a pulse output with a desired duty cycle. The control bits are set as follows:

1. In TCR, clear bit CCLR1 to 0 and set bit CCLR0 to 1 so that TCNT is cleared at a TCORA compare match.
2. In TCSR, set bits OS3 to OS0 to B'0110, causing the output to change to 1 at a TCORA compare match and to 0 at a TCORB compare match.

With these settings, the 8-bit timer provides pulses output at a cycle determined by TCORA with a pulse width determined by TCORB. No software intervention is required. The output level of the 8-bit timer holds 0 until the first compare match occurs after a reset.

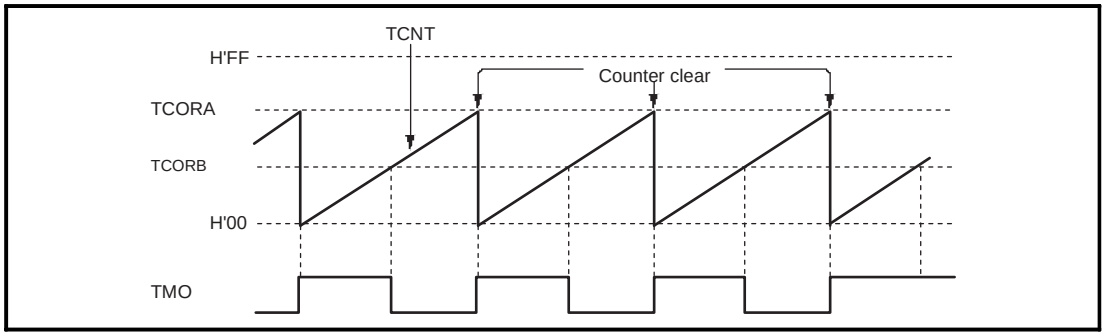



**Figure 11.3 Example of Pulse Output**

### 11.4.2 ResetInput

Figure 11.4 shows an example of the 8-bit timer being used to generate a pulse which is output after a desired delay time from a TMRI input. The control bits are set as follows:

1. Set both bits CCLR1 and CCLR0 in TCR to 1 and set the TMRIS bit in TCCR to 1 so that TCNT is cleared at the high level input of the TMRI signal.
2. In TCSR, set bits OS3 to OS0 to B'0110, causing the output to change to 1 at a TCORA compare match and to 0 at a TCORB compare match.

With these settings, the 8-bit timer provides pulses output at a desired delay time from a TMRI input determined by TCORA and with a pulse width determined by TCORB and TCORA.

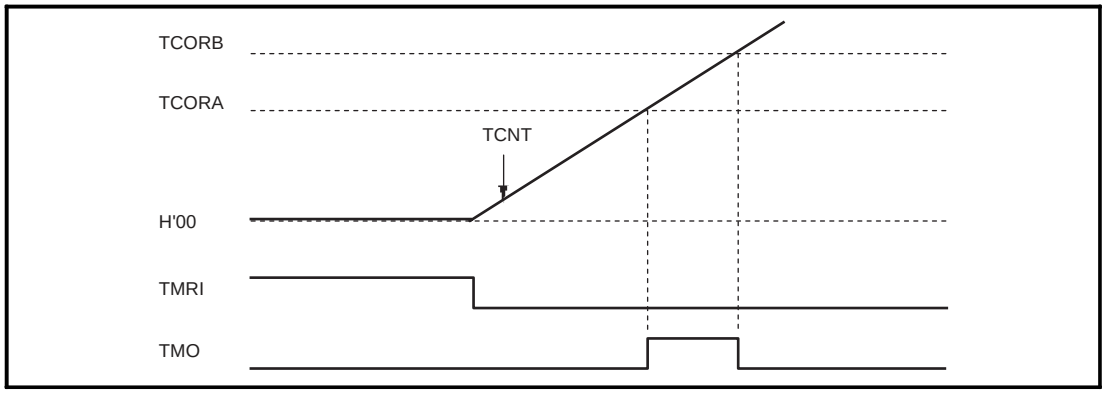



**Figure 11.4 Example of Reset Input**

## 11.5 Operation Timing

### 11.5.1 TCNT Count Timing

Figure 11.5 shows the TCNT count timing for internal clock input. Figure 11.6 shows the TCNT count timing for external clock input. Note that the external clock pulse width must be at least 1.5 states for incrementation at a single edge, and at least 2.5 states for incrementation at both edges. The counter will not increment correctly if the pulse width is less than these values.

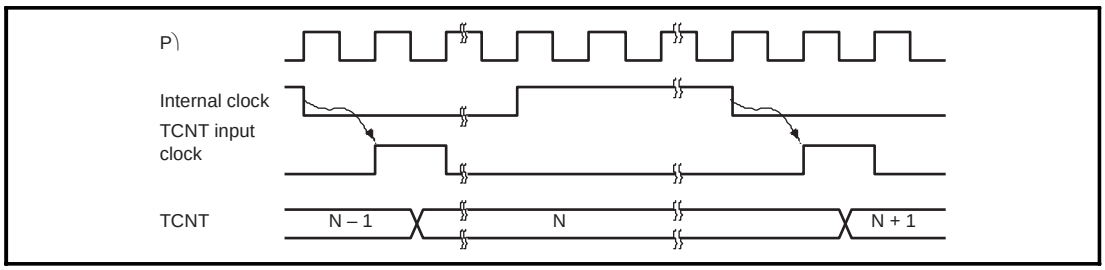



**Figure 11.5 Count Timing for Internal Clock Input at Falling Edge**

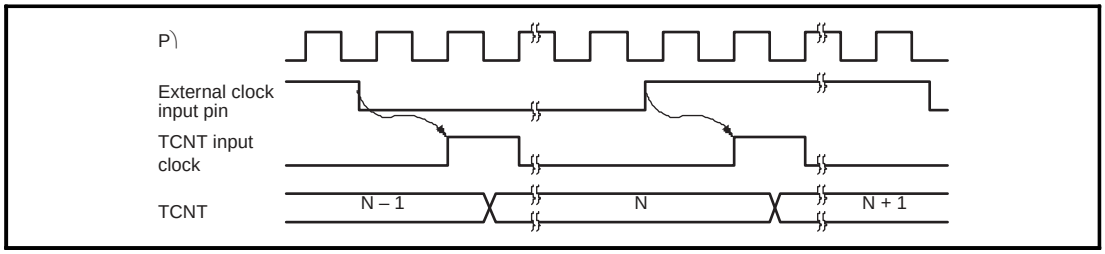



**Figure 11.6 Count Timing for External Clock Input at Falling and Rising Edges**

### 11.5.2 Timing of CMFA and CMFB Setting at Compare Match

The CMFA and CMFB flags in TCSR are set to 1 by a compare match signal generated when the TCOR and TCNT values match. The compare match signal is generated at the last state in which the match is true, just before the timer counter is updated. Therefore, when the TCOR and TCNT values match, the compare match signal is not generated until the next TCNT clock input. Figure 11.7 shows this timing.

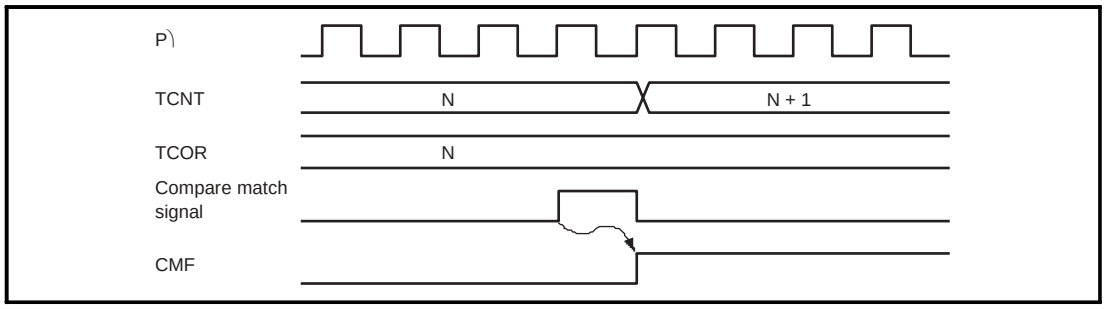



**Figure 11.7 Timing of CMF Setting at Compare Match**

### 11.5.3 Timing of Timer Output at Compare Match

When a compare match signal is generated, the timer output changes as specified by bits OS3 to OS0 in TCSR. Figure 11.8 shows the timing when the timer output is toggled by the compare match A signal.

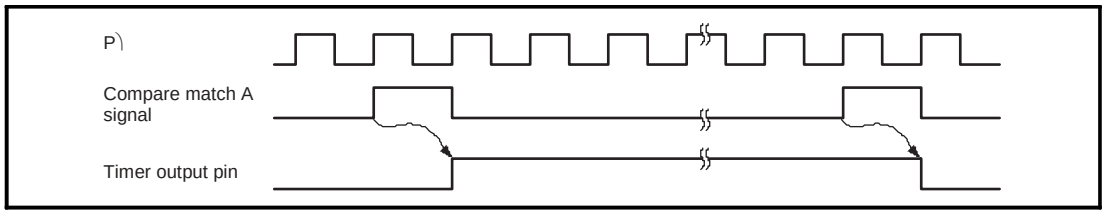



**Figure 11.8 Timing of Toggled Timer Output at Compare Match A**

### 11.5.4 Timing of Counter Clear by Compare Match

TCNT is cleared when compare match A or B occurs, depending on the settings of bits CCLR1 and CCLR0 in TCR. Figure 11.9 shows the timing of this operation.

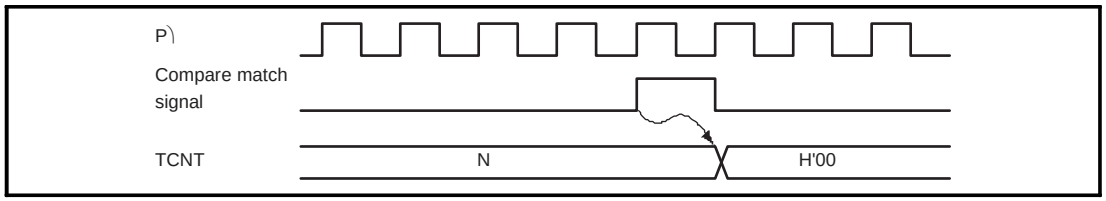



**Figure 11.9 Timing of Counter Clear by Compare Match**

### 11.5.5 Timing of TCNT External Reset

TCNT is cleared at the rising edge or high level of an external reset input, depending on the settings of bits CCLR1 and CCLR0 in TCR. The clear pulse width must be at least 2 states. Figures 11.10 and 11.11 show the timing of this operation.

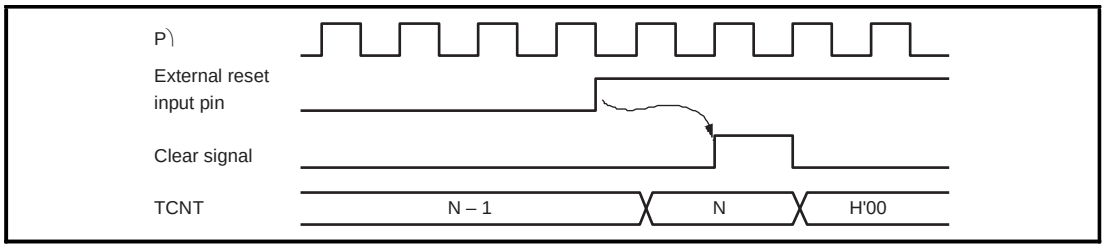



**Figure 11.10 Timing of Clearance by External Reset (Rising Edge)**

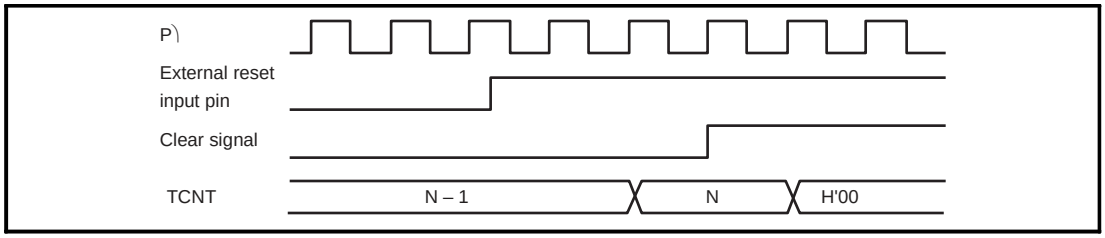



**Figure 11.11 Timing of Clearance by External Reset (High Level)**

### 11.5.6 Timing of Overflow Flag (OVF) Setting

The OVF bit in TCSR is set to 1 when TCNT overflows (changes from H'FF to H'00). Figure 11.12 shows the timing of this operation.

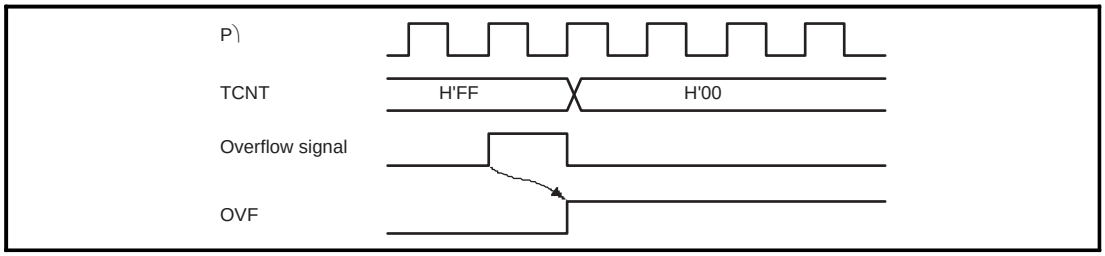



**Figure 11.12 Timing of OVF Setting**

## 11.6 Operation with Cascaded Connection

If bits CKS2 to CKS0 in either TCR_0 or TCR_1 are set to B'100, the 8-bit timers of the two channels are cascaded. With this configuration, a single 16-bit timer could be used (16-bit counter mode) or compare matches of the 8-bit channel 0 could be counted by the timer of channel 1 (compare match count mode).

### 11.6.1 16-Bit Counter Mode

When bits CKS2 to CKS0 in TCR_0 are set to B'100, the timer functions as a single 16-bit timer with channel 0 occupying the upper 8 bits and channel 1 occupying the lower 8 bits.

**(1) Setting of Compare Match Flags:**

The CMF flag in TCSR_0 is set to 1 when a 16-bit compare match event occurs.

The CMF flag in TCSR_1 is set to 1 when a lower 8-bit compare match event occurs.

**(2) Counter Clear Specification**

If the CCLR1 and CCLR0 bits in TCR_0 have been set for counter clear at compare match, the 16-bit counter (TCNT_0 and TCNT_1 together) is cleared when a 16-bit compare match event occurs. The 16-bit counter (TCNT0 and TCNT1 together) is cleared even if counter clear by the TMRI0 pin has been set.

The settings of the CCLR1 and CCLR0 bits in TCR_1 are ignored. The lower 8 bits cannot be cleared independently.

**(3) Pin Output**

Control of output from the TMO0 pin by bits OS3 to OS0 in TCSR_0 is in accordance with the 16-bit compare match conditions.

Control of output from the TMO1 pin by bits OS3 to OS0 in TCSR_1 is in accordance with the lower 8-bit compare match conditions.

### 11.6.2 Compare Match Count Mode

When bits CKS2 to CKS0 in TCR_1 are set to B'100, TCNT_1 counts compare match A for channel 0. Channels 0 and 1 are controlled independently. Conditions such as setting of the CMF flag, generation of interrupts, output from the TMO pin, and counter clear are in accordance with the settings for each channel.

## 11.7 Interrupt Sources

### 11.7.1 Interrupt Sources and DTC Activation

There are three interrupt sources for the 8-bit timer (TMR_0 or TMR_1): CMIA, CMIB, and OVI. Their interrupt sources and priorities are shown in table 11.3. Each interrupt source is enabled or disabled by the corresponding interrupt enable bit in TCR or TCSR, and independent interrupt requests are sent for each to the interrupt controller. It is also possible to activate the DTC by means of CMIA and CMIB interrupts.

**Table 11.3 8-Bit Timer (TMR_0 or TMR_1) Interrupt Sources**

| Name | Interrupt Source | Interrupt Flag | DTC Activation | Priority |
|---|---|---|---|---|
| CMIA0 | TCORA_0 compare match | CMFA | Possible (VNUM = 2'b00) | High |
| CMIB0 | TCORB_0 compare match | CMFB | Possible (VNUM = 2'b01) | |
| OVI0 | TCNT_0 overflow | OVF | Not possible | Low |
| CMIA1 | TCORA_1 compare match | CMFA | Possible (VNUM = 2'b10) | High |
| CMIB1 | TCORB_1 compare match | CMFB | Possible (VNUM = 2'b11) | |
| OVI1 | TCNT_1 overflow | OVF | Not possible | Low |

Note: VNUM is an internal signal.

### 11.7.2 A/D Converter Activation

The A/D converter can be activated only by TMR_0 compare match A.

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 by the occurrence of TMR_0 compare match A, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

## 11.8 Usage Notes

### 11.8.1 Notes on Setting Cycle

If the compare match is selected for counter clear, TCNT is cleared at the last state in the cycle in which the values of TCNT and TCOR match. TCNT updates the counter value at this last state. Therefore, the counter frequency is obtained by the following formula.

$$f = \phi / (N + 1)$$

f: Counter frequency
$\phi$: Operating frequency
N: TCOR value

### 11.8.2 Conflict between TCNT Write and Clear

If a counter clear signal is generated during the $T_2$ state of a TCNT write cycle, the clear takes priority and the write is not performed as shown in figure 11.13.

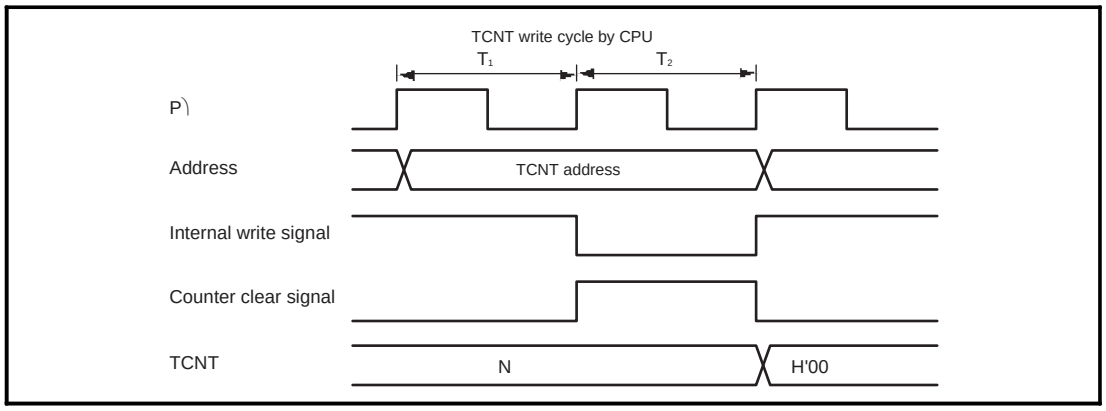



**Figure 11.13 Conflict between TCNT Write and Clear**

### 11.8.3 Conflict between TCNT Write and Increment

If a TCNT input clock pulse is generated during the $T_2$ state of a TCNT write cycle, the write takes priority and the counter is not incremented as shown in figure 11.14.

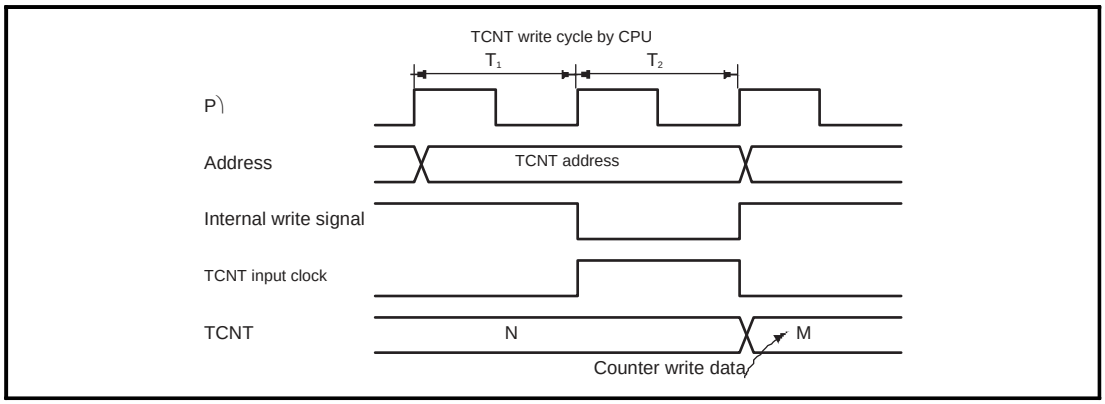



**Figure 11.14 Conflict between TCNT Write and Increment**

### 11.8.4 Conflict between TCOR Write and Compare Match

If a compare match event occurs during the $T_2$ state of a TCOR write cycle, the TCOR write takes priority and the compare match signal is inhibited as shown in figure 11.15.

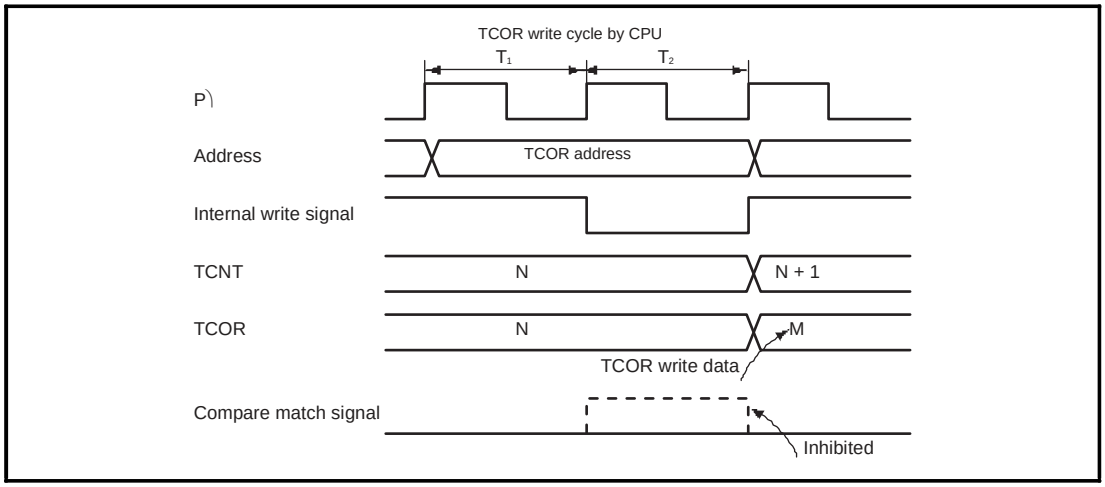



**Figure 11.15 Conflict between TCOR Write and Compare Match**

### 11.8.5 Conflict between Compare Matches A and B

If compare match events A and B occur at the same time, the 8-bit timer operates in accordance with the priorities for the output statuses set for compare match A and compare match B, as shown in table 11.4.

**Table 11.4 Timer Output Priorities**

| Output Setting | Priority |
|---|---|
| Toggle output | High |
| 1-output |  |
| 0-output | |
| No change | Low |

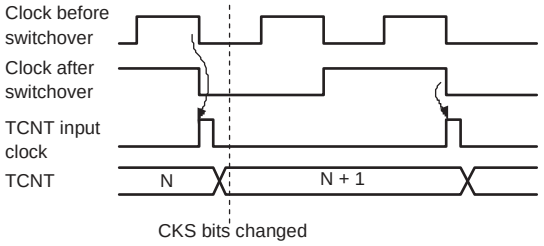
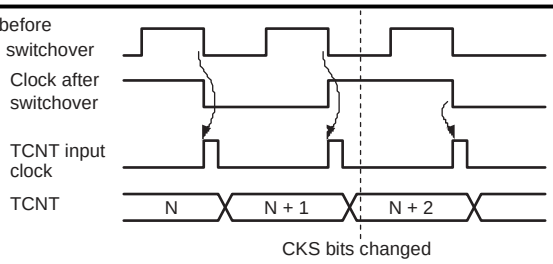
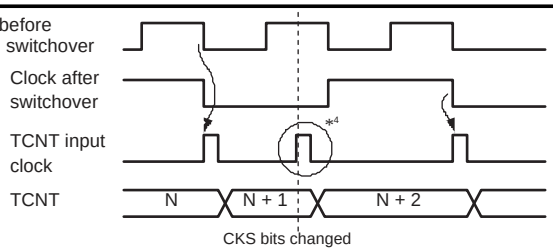
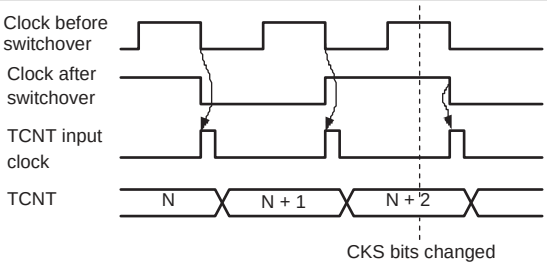
### 11.8.6 Switching of Internal Clocks and TCNT Operation

TCNT may be incremented erroneously depending on when the internal clock is switched. Table 11.5 shows the relationship between the timing at which the internal clock is switched (by writing to bits CKS1 and CKS0) and the TCNT operation.

When the TCNT clock is generated from an internal clock, the rising or falling edge of the internal clock pulse are always monitored. Table 11.5 assumes that the falling edge is selected. If the signal levels of the clocks before and after switching change from high to low as shown in item 3, the change is considered as the falling edge. Therefore, a TCNT clock pulse is generated and TCNT is incremented. This is similar to when the rising edge is selected.

The erroneous incrementation of TCNT can also happen when switching between rising and falling edges of the internal clock, and when switching between internal and external clocks.

**Table 11.5 Switching of Internal Clock and TCNT Operation**

| No. | Timing to Change CKS1 and CKS0 Bits | TCNT Clock Operation |
|---|---|---|
| 1 | Switching from low to low*[1] |   |
| 2 | Switching from low to high*[2] |   |
| 3 | Switching from high to low*[3] |   |
| 4 | Switching from high to high |   |

Notes: 1. Includes switching from low to stop, and from stop to low.

2. Includes switching from stop to high.
3. Includes switching from high to stop.
4. Generated because the change of the signal levels is considered as a falling edge; TCNT is incremented.

### 11.8.7 Mode Settingwith Cascaded Connection

If 16-bit counter mode and compare match count mode are specified at the same time, input clocks for TCNT_0 and TCNT_1 are not generated, and the counter stops. Do not specify 16-bit counter mode and compare match count mode simultaneously.

### 11.8.8 Module Stop State Setting

Operation of the TMR can be disabled or enabled using the module stop control register. The initial setting is for operation of the TMR to be halted. Register access is enabled by clearing module stop state. For details, see section 18, Power-Down States.

### 11.8.9 Interrupts in Module Stop State

If module stop state is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DTC activation source. Interrupts should therefore be disabled before entering module stop state.