High Speed NAND Flash Memory

MT29H8G08ACAH1, MT29H16G08ECAH1, MT29H32G08GCAH2

Features

- Open NAND Flash Interface (ONFI) 2.0 compliant[1]
- Single-level cell (SLC) technology
- Organization:
  - Page size x8: 4,320 bytes (4,096 + 224 bytes)
  - Block size: 128 pages (512K + 28K bytes)
  - Plane size: 4 planes × 512 blocks per plane
  - Device size: 8Gb: 2,048 blocks; 16Gb: 4,096 blocks; 32Gb: 8,192 blocks
- I/O Read performance:
  - Clock rate: 12ns (DDR)
  - Read throughput per pin: 166MT/s
  - SET FEATURES selects asynchronous/DDR mode for data output
- I/O Write performance:
  - Clock rate: 12ns (DDR)
  - Loading throughput per pin: 166MT/s
  - SET FEATURES selects asynchronous/DDR mode for data input
  - Command/Address entry on rising edge of CLK
- Array performance
  - Single-Plane Read Page: 25µs (MAX)
  - Multi-Plane Read Page: 30µs (MAX)
  - Program Page: 160µs (TYP)
  - Erase Block: 3ms (TYP)
- Operating Voltage Range
  - V_{CC}: 2.7-3.6V
  - V_{CCQ}: 1.7-1.95V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set:
  - Program Cache
  - Read Cache Sequential
  - Read Cache Random
  - One-time programmable (OTP) mode
  - Multi-plane commands
  - Multi-LUN operations
  - Read Unique ID
  - Copyback
- Operation status byte provides software method for detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data I/O in the synchronous interface
- Copyback operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles[2]
  - Operating temperature:
    Commercial: 0 °C to +70 °C
    Wireless: –25 °C to +85 °C
- First block (block address 00h) is valid with ECC[2]
- Package: 100-ball BGA
- RESET (FFh) required as first command after power-on

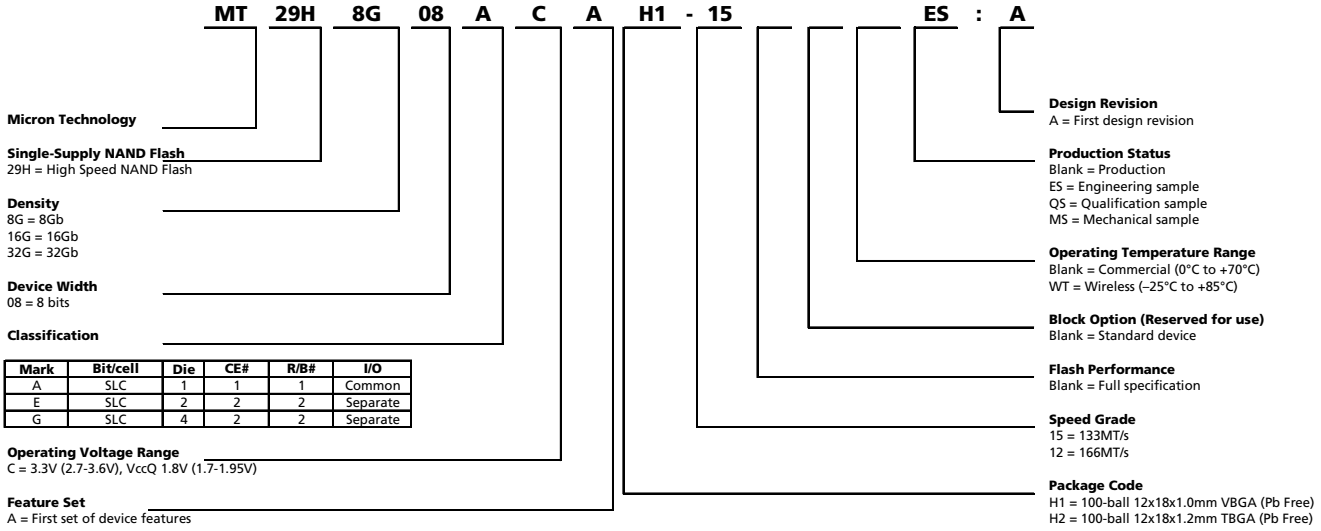
[1] The ONFI 2.0 specification is available at http://www.onfi.org/.

[2] For further details, see “Error Management” on page 74.

Part Numbering Information

Micron NAND Flash devices are available in several different configurations and densities (see Figure 1).

Figure 1: Part Number Chart



Mark	Bit/cell	Die	CE#	R/B#	I/O
A	SLC	1	1	1	Common
E	SLC	2	2	2	Separate
G	SLC	4	2	2	Separate

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part is offered and valid by using the Micron Parametric Part Search Web Site at: http://www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

Table of Contents

List of Figures

List of Tables

General Description

Micron High Speed NAND Flash technology provides high-performance NAND Flash memory with an interface that supports up to 166MB/s data read and write throughput.

Micron High Speed NAND Flash devices include two data interfaces—a synchronous interface for high-performance I/O operations, and an asynchronous interface for legacy NAND Flash applications. These devices use a highly multiplexed 8-bit bus (DQ[7:0]) to transfer commands, addresses, and data. Data transfers in the synchronous interface include a bidirectional data strobe (DQS). Between the synchronous and asynchronous interfaces there are five control signals that are used to implement the NAND Flash protocol. In the synchronous interface these signals are CE#, CLE, ALE, CLK, and W/R#; in the asynchronous interface these signals are CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

A logical unit (LUN), or die, is the minimum unit that can independently execute commands and report status. There is at least one LUN per CE#. Each LUN contains four planes. Each plane consists of 512 blocks. Each block is subdivided into 128 programmable pages. Each page consists of 4,320 bytes.

The contents of each page can be programmed in tPROG, and an entire block can be erased in tBERS. PROGRAM/ERASE endurance is specified at 100,000 cycles when using appropriate error correction code (ECC), wear leveling, and error management.

Figure 2: Ball Assignment (Top View) 100-Ball VBGA Single x8 (MT29H8G08ACAH1)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC									NC
C										
D		RFU	DNU	NC	NC	NC	NC	DNU	RFU	
E		RFU	DNU	NC	WP#	NC	NC	DNU	RFU	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	RFU	RFU	NC	NC	VCCQ	VSSQ	
J		NC	NC	NC	NC	R/B#	NC	NC	NC	
K		DQ0	DQ2	ALE	NC	NC	CE#	DQ5	DQ7	
L		VCCQ	VSSQ	VCCQ	NC	NC	VCCQ	VSSQ	VCCQ	
M		NC	NC	VSSQ	CLE	RE# (W/R#)	VSSQ	NC	NC	
N		DQ1	DQ3	RFU	NC	RFU	NC	DQ4	DQ6	
P		VSSQ	VCCQ	RFU	N/A[1] (DQS)	RFU	WE# (CLK)	VCCQ	VSSQ	
R										
T	NC									NC
U	NC	NC							NC	NC

1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Signal names in parentheses are the signal names when the synchronous interface is active.

Figure 3: Ball Assignment (Top View) 100-Ball VBGA/TBGA Dual x8 (MT29H16G08ECAH1, MT29H32G08GCAH2)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC									NC
C										
D		RFU	DNU	NC	WP#-2	NC	NC	DNU	RFU	
E		RFU	DNU	NC	WP#-1	NC	NC	DNU	RFU	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	RFU	RFU	R/B2#	NC	VCCQ	VSSQ	
J		DQ0-2	DQ2-2	ALE-2	NC	R/B#	NC	DQ5-2	DQ7-2	
K		DQ0-1	DQ2-1	ALE-1	NC	CE2#	CE#	DQ5-1	DQ7-1	
L		VCCQ	VSSQ	VCCQ	CLE-2	RE#-2 (W/R#-2)	VCCQ	VSSQ	VCCQ	
M		DQ1-2	DQ3-2	VSSQ	CLE-1	RE#-1 (W/R#-1)	VSSQ	DQ4-2	DQ6-2	
N		DQ1-1	DQ3-1	RFU	N/A[1] (DQS-2)	RFU	WE#-2 (CLK-2)	DQ4-1	DQ6-1	
P		VSSQ	VCCQ	RFU	N/A[1] (DQS-1)	RFU	WE#-1 (CLK-1)	VCCQ	VSSQ	
R										
T	NC									NC
U	NC	NC							NC	NC

1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Signal names in parentheses are the signal names when the synchronous interface is active.

Table 1: Signal Definitions

Symbol[1]		Type	Description[2]
Async	**Sync**		
ALE, ALE-1, ALE-2	ALE, ALE-1, ALE-2	Input	**Address latch enable:** Loads an address from DQ[7:0] into the address register.
CE#, CE2#	CE#, CE2#	Input	**Chip enable:** An asynchronous-only signal that enables or disables one or more logical units. For the 16Gb device, CE# controls the first 8Gb of memory ("-1"); CE2# controls the second 8Gb of memory ("-2"). For the 32Gb device, CE# controls the first 16Gb of memory ("-1"); CE2# controls the second 16Gb of memory ("-2").
CLE, CLE-1, CLE-2	CLE, CLE-1, CLE-2	Input	**Command latch enable:** Loads a command from DQ[7:0] into the command register.
DQ[7:0], DQ[7:0]-1, DQ[7:0]-2	DQ[7:0], DQ[7:0]-1, DQ[7:0]-2	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
N/A	DQS, DQS-1, DQS-2	I/O	**Data strobe:** Provides a synchronous clock reference for data input and output.
RE#, RE#-1, RE#-2	W/R#, W/R#-1, W/R#-2	Input	**Read enable and Write/Read#:** RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQ[7:0] and DQS.
WE#, WE#-1, WE#-2	CLK, CLK-1, CLK-2	Input	**Write enable and Clock:** WE# transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLK latches command and address cycles.
WP#, WP#-1, WP#-2	WP#, WP#-1, WP#-2	Input	**Write protect:** WP# is an asynchronous-only signal that enables or disables array program and erase operations.
R/B#, R/B2#	R/B#, R/B2#	Output	**Ready/Busy#:** An open-drain, active-low output that requires an external pull-up resistor.
Vcc	Vcc	Supply	**Vcc:** Power supply for core
VccQ	VccQ	Supply	**VccQ:** Power supply for I/Os
Vss	Vss	Supply	**Vss:** Ground connection for core
VssQ	VssQ	Supply	**VssQ:** Ground connection for I/Os
NC	NC	—	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU	—	**Do not use:** DNUs must be left unconnected.
RFU	RFU	—	**Reserved for future use:** RFUs must be left unconnected.

1. See "Device and Array Organization" on page 13 for detailed signal connections for each LUN.
2. See "Bus Operation" beginning on page 16 for detailed asynchronous and synchronous interface signal-use explanations.

Architecture

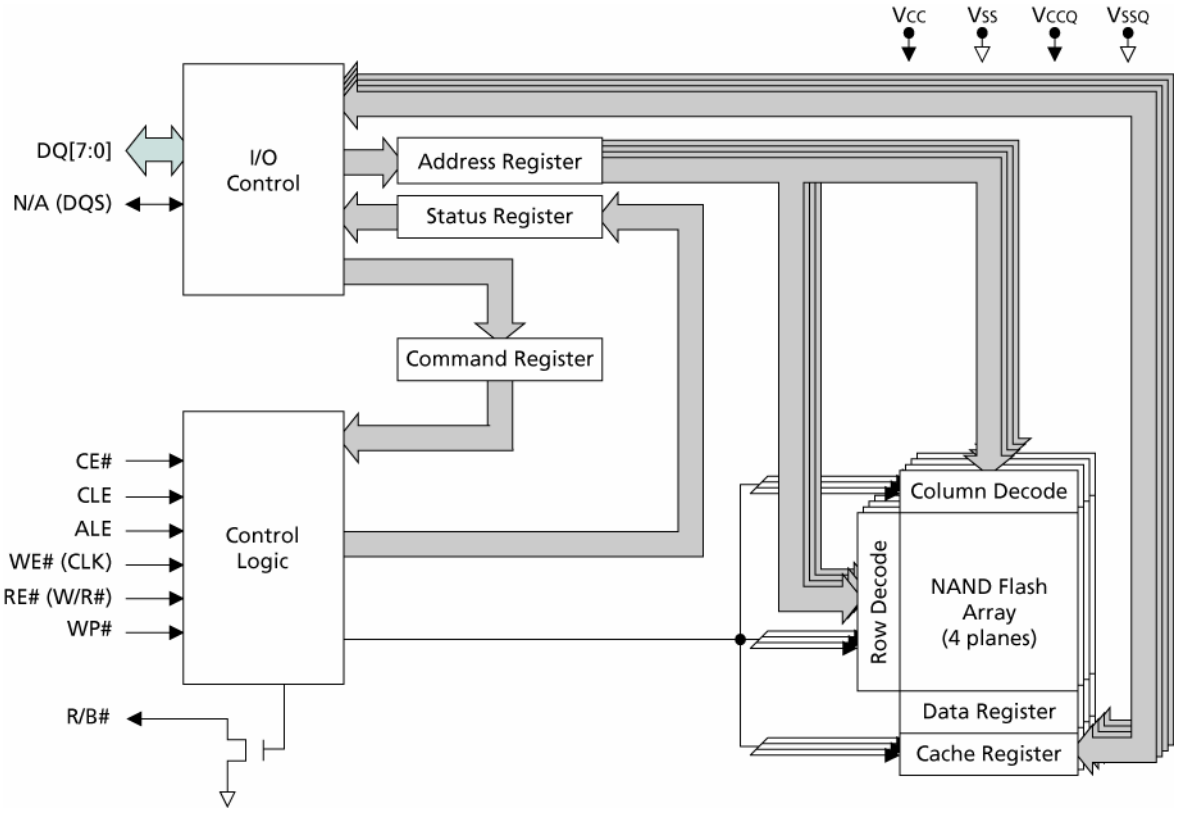
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address or to a column decoder to select a column address.

The data are transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for NAND Flash memory array operation.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations the data and cache registers operate independently to increase data throughput.

The status register reports the status of LUN operation.

Figure 4: High Speed NAND Flash LUN Functional Block Diagram



Addressing and Memory Map

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence shown in Table 2 on page 15.

Device and Array Organization

Figure 5: Device Organization for MT29H8G08ACAH1

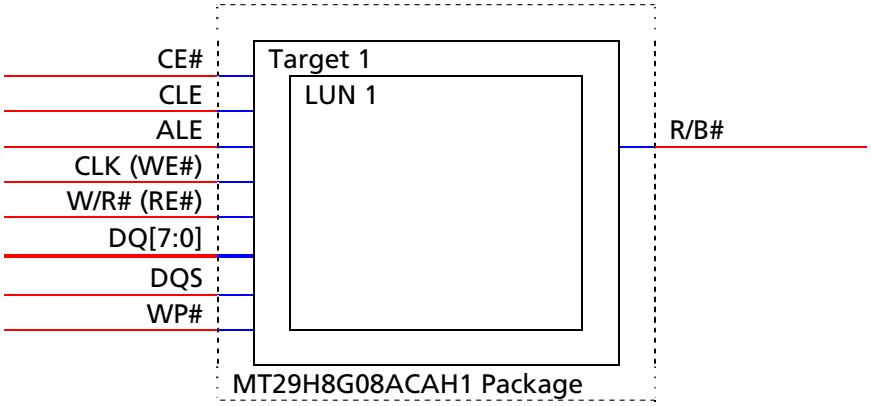


Figure 6: Device Organization for MT29H16G08ECAH1

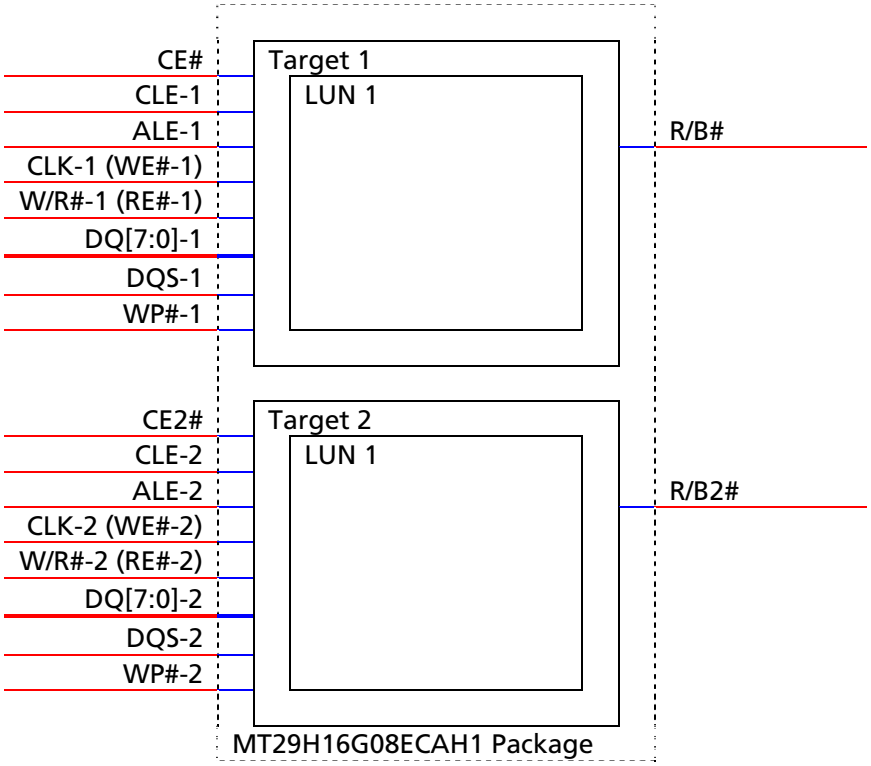


Figure 7: Device Organization for MT29H32G08GCAH2

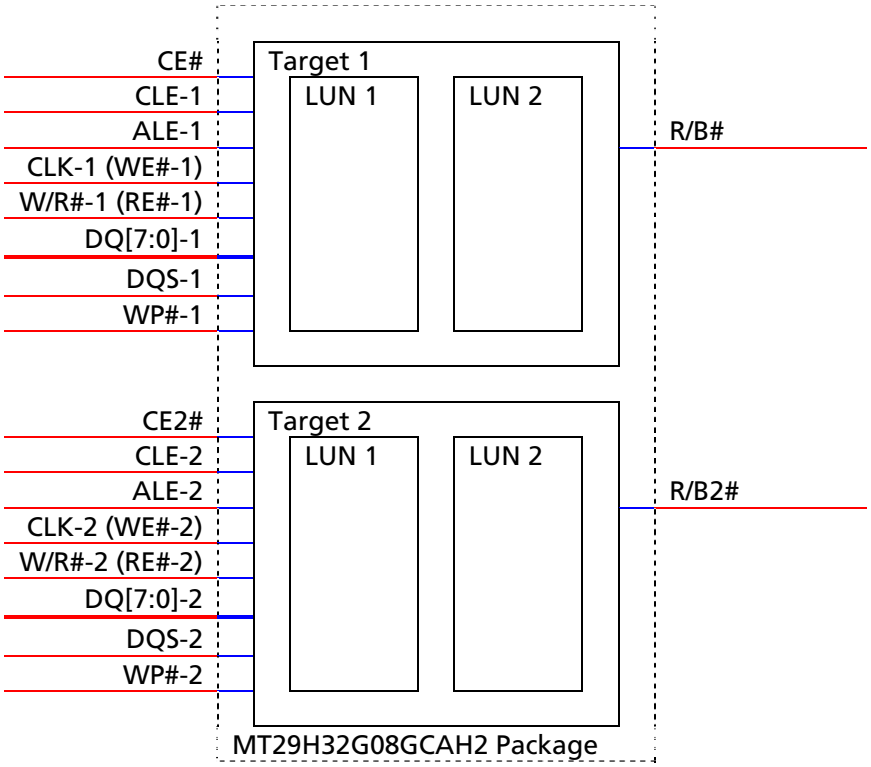


Figure 8: Array Organization for 8Gb Logical Unit (LUN)

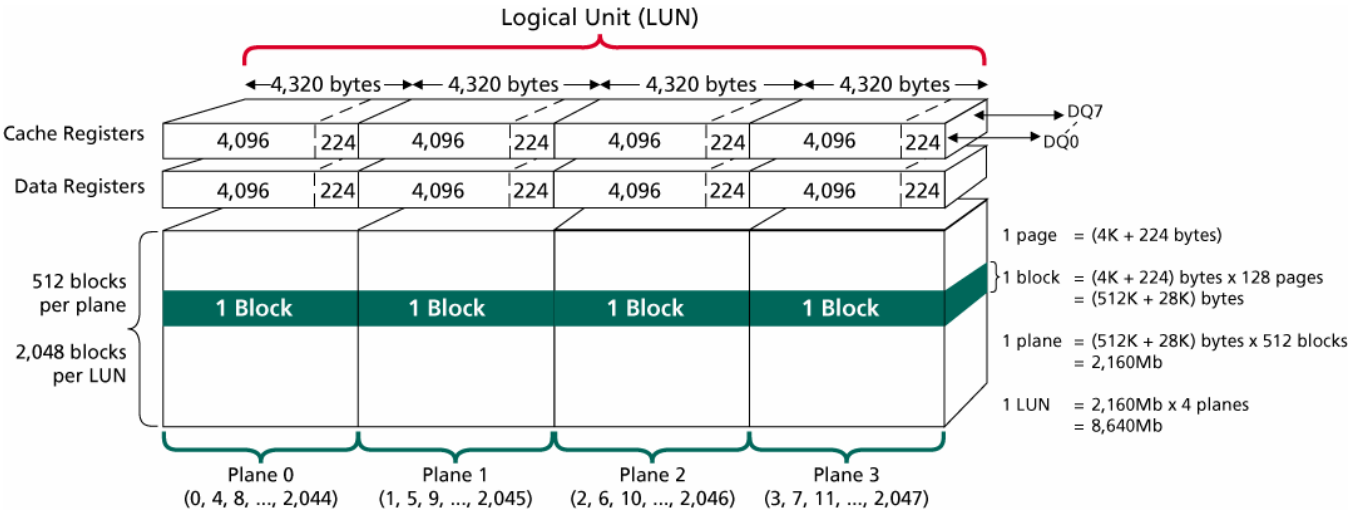


Table 2: Array Addressing

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7[4]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8[4]
Fifth	LOW	LOW	LOW	LOW	LOW	LA0[5]	BA17	BA16

1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
2. When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns an even byte and an odd byte.
3. Column addresses between 4,320 (10E0h) and 8,191 (1FFFh) are invalid.
4. BA[8:7] are the plane-select bits:
   Plane 0: BA[8:7] = "00"
   Plane 1: BA[8:7] = "01"
   Plane 2: BA[8:7] = "10"
   Plane 3: BA[8:7] = "11"
5. LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise it should be held LOW.
   LUN 0: LA0 = "0"
   LUN 1: LA0 = "1"

Bus Operation

MT29H-series NAND Flash devices have two interfaces: a synchronous interface for fast data I/O transfer and an asynchronous interface that is backwards compatible with existing NAND Flash devices.

The NAND Flash command protocol for both the asynchronous and synchronous interfaces is identical, however there are some differences issuing command, address, and data I/O cycles using the NAND Flash signals.

Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on to provide compatibility with existing NAND controllers that may not support the synchronous interface. The DQS signal is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized in Table 3.

Table 3: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQx	DQS[1]	WP#
Standby	H	X	X	X	X	X	X	0V/VccQ[2]
Bus idle	L	X	X	H	H	X	X	X
Command input	L	H	L	⎍	H	X	X	H
Address input	L	L	H	⎍	H	X	X	H
Data input	L	L	L	⎍	H	X	X	H
Data output	L	L	L	H	⎎	output	X	X
Write protect	X	X	X	X	X	X	X	L

1. DQS is tri-stated when the asynchronous interface is active.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

Asynchronous Enable / Standby

CE# is used to enable a target. When CE# is driven LOW all of the signals for that target are enabled. With CE# LOW, the target can now accept commands, addresses, and data I/O. There may be more than one target in a NAND package. Each target is controlled by its own CE#; the first target is controlled by CE#; the second target (if present) is controlled by CE2#, etc.

A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. This allows the NAND Flash to share the same memory bus as other Flash or SRAM devices. While the target is disabled, other devices on the memory bus can be accessed.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the LUNs complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when:

- CE# is LOW,
- WE# is HIGH, and
- RE# is HIGH.

During bus idle all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.

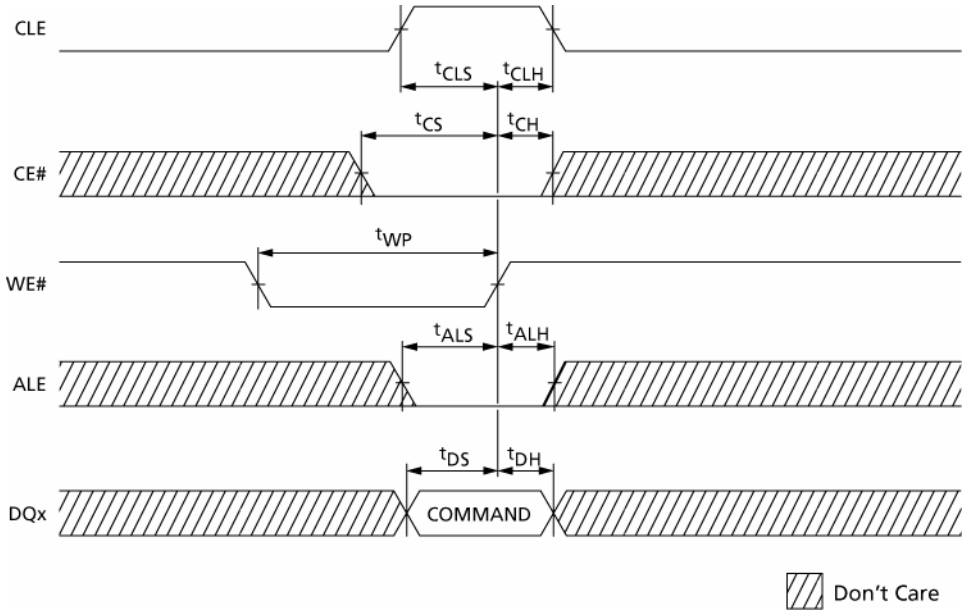
Asynchronous Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when:

- CE# is LOW,
- ALE is LOW,
- CLE is HIGH, and
- RE# is HIGH.

Commands are typically ignored by LUNs that are busy; however, some commands, like READ STATUS (70h) and SELECT LUN WITH STATUS (78h), are accepted by LUNs even when they are busy.

Figure 9: Command Latch Cycle



Asynchronous Addresses

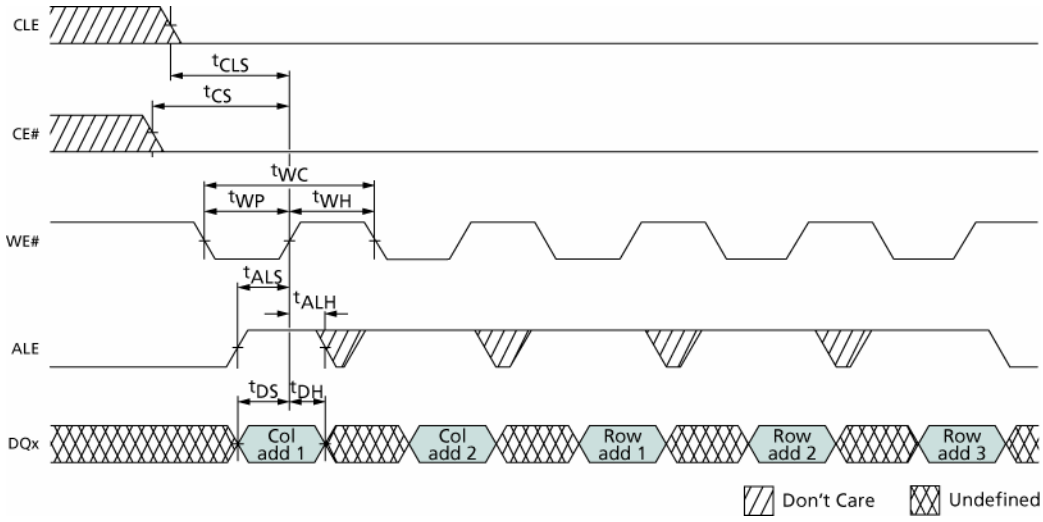
An address is written from DQ[7:0] to the address register on the rising edge of WE# when:

- CE# is LOW,
- ALE is HIGH,
- CLE is LOW, and
- RE# is HIGH.

Bits not part of the address space must be LOW (see Table 2 on page 15). The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see "Command Definitions" on page 34).

Addresses are typically ignored by LUNs that are busy; however, some addresses are accepted by LUNs even when they are busy, like address cycles that follow the SELECT LUN WITH STATUS (78h) command.

Figure 10: Address Latch Cycle



Asynchronous Data Input

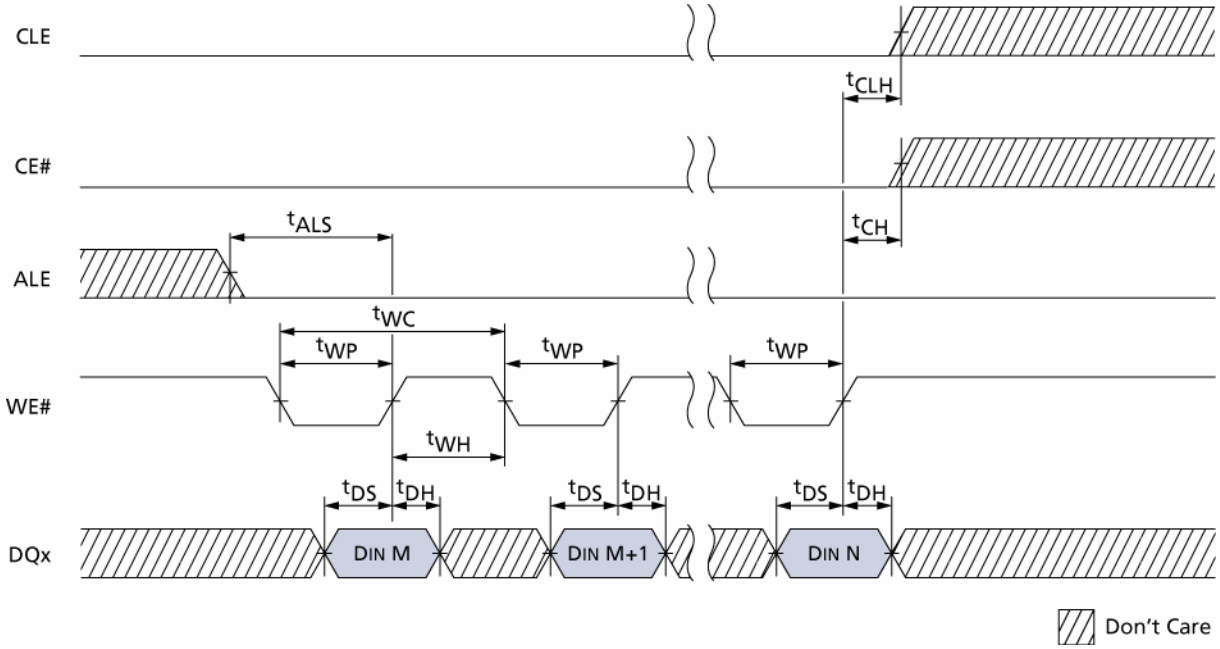
Data is written from DQ[7:0] to the cache register of the selected LUN on the rising edge of WE# when:

- CE# is LOW,
- ALE is LOW,
- CLE is LOW, and
- RE# is HIGH.

Data input is ignored by LUNs that are not selected or are busy, except if the LUN is busy with a PROGRAM PAGE CACHE MODE operation.

See Figure 11 on page 19.

Figure 11: Data Input Cycles



Asynchronous Data Output

Data can be output from a LUN if it is ready. Data output is permitted following a READ operation from the NAND Flash array.

Data is output from the cache register of the selected LUN to DQ[7:0] on the falling edge of RE# when:

- CE# is LOW,
- ALE is LOW,
- CLE is LOW, and
- WE# is HIGH.

If the host controller is using a tRC of 30ns or greater, the host can latch the data on the rising edge of RE#. See Figure 12 on page 20 for proper timing.

If the host controller is using a tRC that is less than 30ns, the host can latch the data on the next falling edge of RE#. See Figure 13 on page 20 for extended data output (EDO) timing.

To prevent data contention following a Multi-LUN operation, the host must enable only one LUN for data output (see Multi-LUN Operations on page 72). Use the SELECT LUN WITH STATUS (78h) command to select the LUN that is to output data. Then issue the READ MODE (00h) command. Data can now be output from the selected LUN.

Data output requests are typically ignored by a LUN that is busy; however, it is permissible to output data from the status register even when a LUN is busy by first issuing the READ STATUS or SELECT LUN WITH STATUS (78h) command.

Figure 12: Data Output Cycles

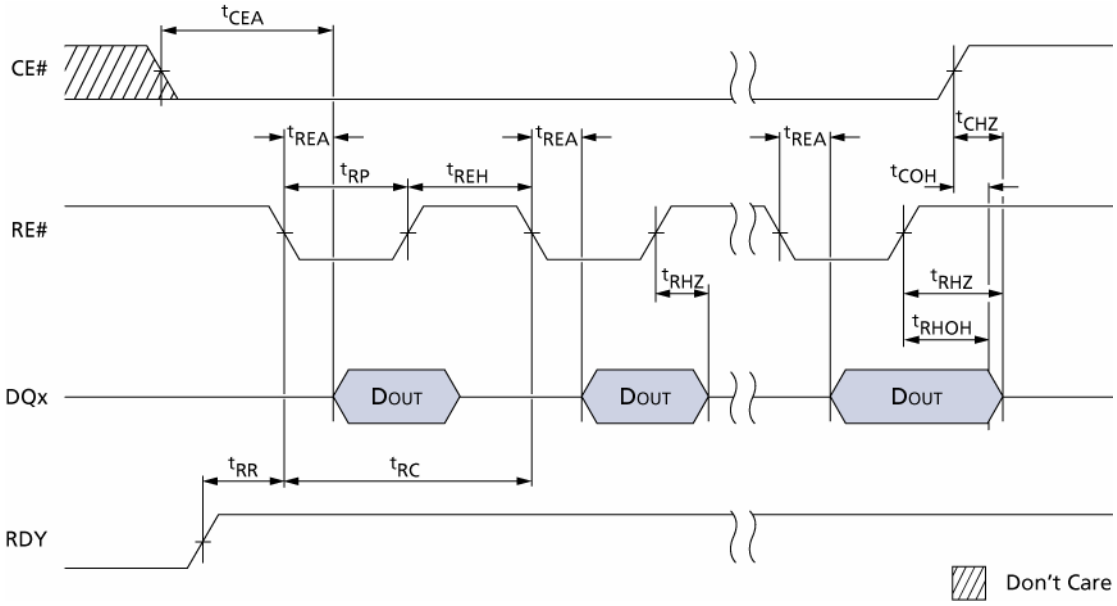
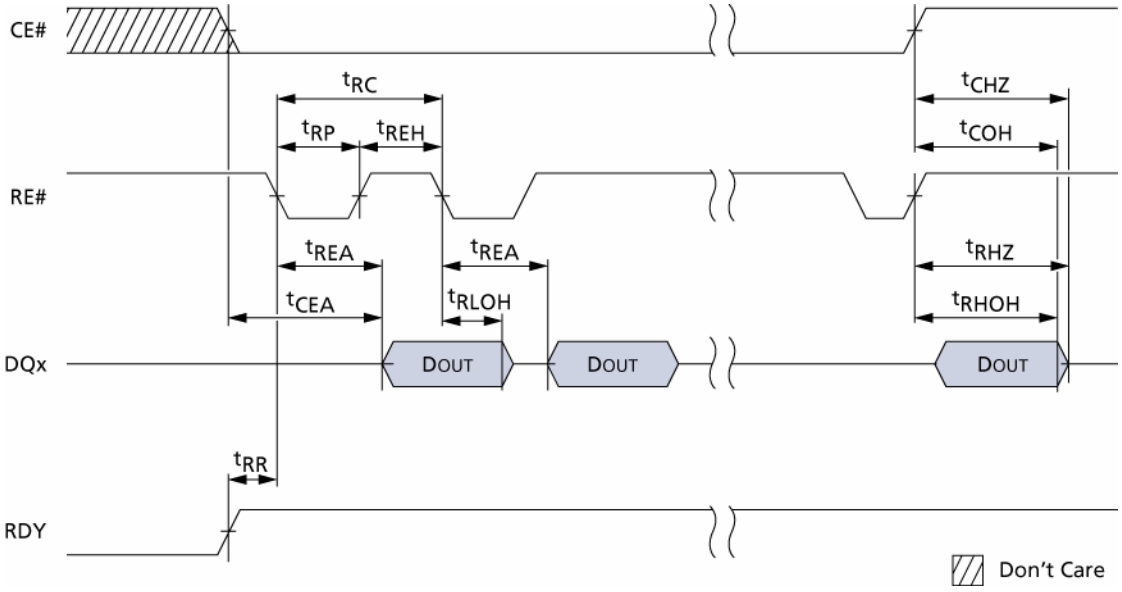


Figure 13: Data Output Cycles (EDO Mode)



Write Protect

The WP# signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc and VccQ are stable to prevent inadvertent PROGRAM and ERASE operations. See "VCC Power Cycling" on page 30 for additional details.

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned the host must wait tWW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The R/B# signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its LUNs are busy (RDY = "0"). A target is ready when all of its LUNs are ready (RDY = "1"). Because each LUN contains a status register, it is possible to determine the independent status of each LUN by polling its status register instead of using the R/B# signal. See "Status Operations" on page 47 for more details regarding LUN status.

If there is more than one target in the NAND package, R/B# reports the status of the target controlled by CE#; R/B2# reports the status of the target controlled by CE2#, etc.

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically R/B# is connected to an interrupt pin on the system controller (see Figure 15 on page 22).

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

Figure 14: Time Constant

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 17 on page 23.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CCQ}.

Equation 1: Rp Calculation

$$Rp\,(MIN) = \frac{V_{CCQ}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + \sum I_L} = \frac{1.85V}{3mA + \sum I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

Figure 15: READY/BUSY# Open Drain

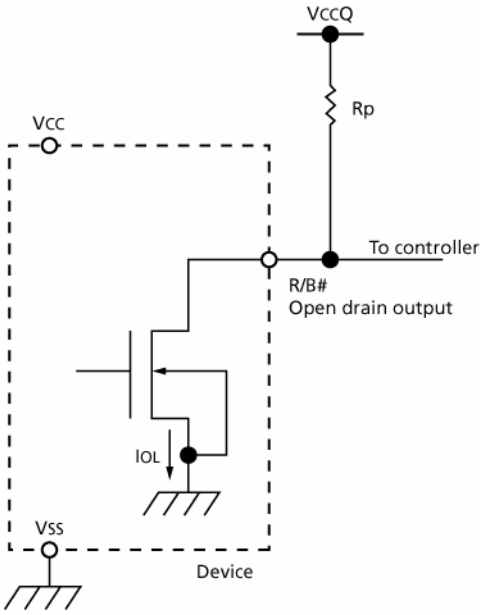
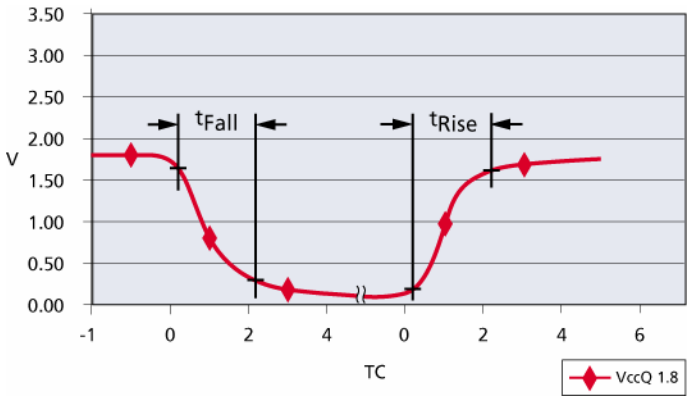
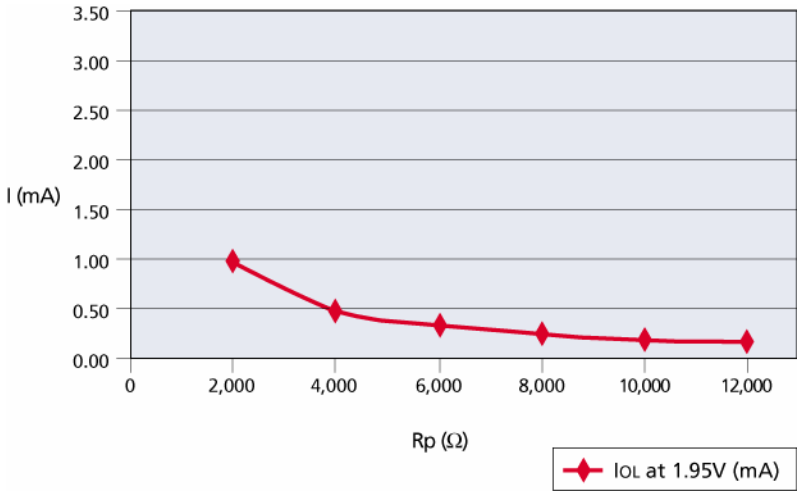


Figure 16: tFall and tRise



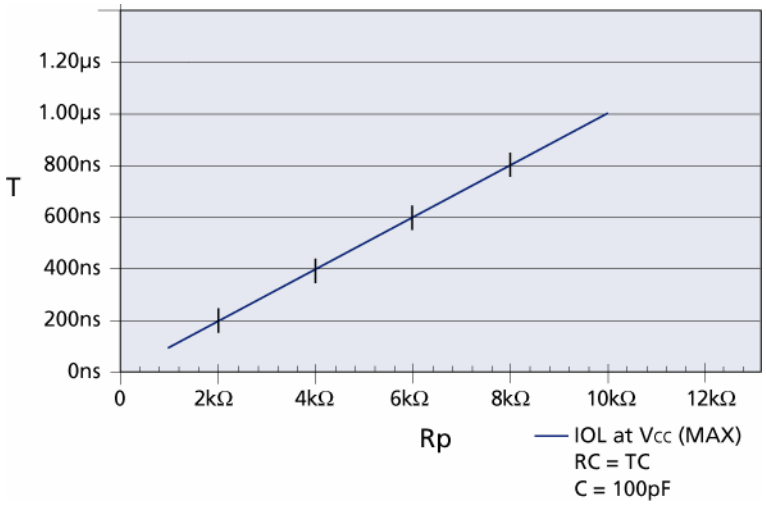
1. tFall and tRise are calculated at 10 percent and 90 percent points.
2. tRise is primarily dependent on external pull-up resistor and external capacitive loading.
3. tFall ≈ 7ns at 1.8V.
4. See TC values in Figure 18 for approximate Rp value and TC.

Figure 17: IOL vs. Rp



1. To calculate Rp, see Equation 1 on page 21.

Figure 18: TC vs. Rp



Synchronous Interface

When the synchronous interface is activated (see "Activating the Synchronous Interface" on page 32) on a target, the target is now capable of high-speed DDR data transfers. Existing signals are redefined for high-speed DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#.

CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output it is driven by the NAND Flash device. During data input it is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, this indicates that the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, this indicates that the NAND Flash is driving the DQ bus and DQS.

The synchronous interface bus modes are summarized in Table 4.

Table 4: Synchronous Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQx	DQS	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/VccQ	1, 2
Bus idle	L	L	L	⌐↑	H	X	X	X	
Bus driving	L	L	L	⌐↑	L	output	output	X	
Command input	L	H	L	⌐↑	H	X	X	H	3
Address input	L	L	H	⌐↑	H	X	X	H	3
Data input	L	H	H	↑↓	H	X	↑↓	H	4
Data output	L	H	H	↑↓	L	output	note 5	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H	⌐↑	L	output	output	X	
Undefined	L	H	L	⌐↑	L	output	output	X	

1. CLK may be stopped when target is disabled, even when R/B# is LOW.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. COMMAND and ADDRESS are latched on the rising edge of CLK.
4. During data input to the device, DQS is the 'clock' that latches the data in the cache register.
5. During data output from the NAND device, DQS is an output generated from CLK after tDQSCK delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

Synchronous Enable / Standby

In addition to the description in "Asynchronous Enable / Standby" section on page 16, the following requirements also apply when the synchronous interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW all of the signals for that target are enabled. The target is not enabled until tCS completes. The target's bus is then idle.

Prior to disabling a target the target's bus must be idle (see "Synchronous Bus Idle / Driving" on page 24). A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK may be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the LUNs complete their operations. Standby helps reduce power consumption.

Synchronous Bus Idle / Driving

A target's bus is idle or driving when:

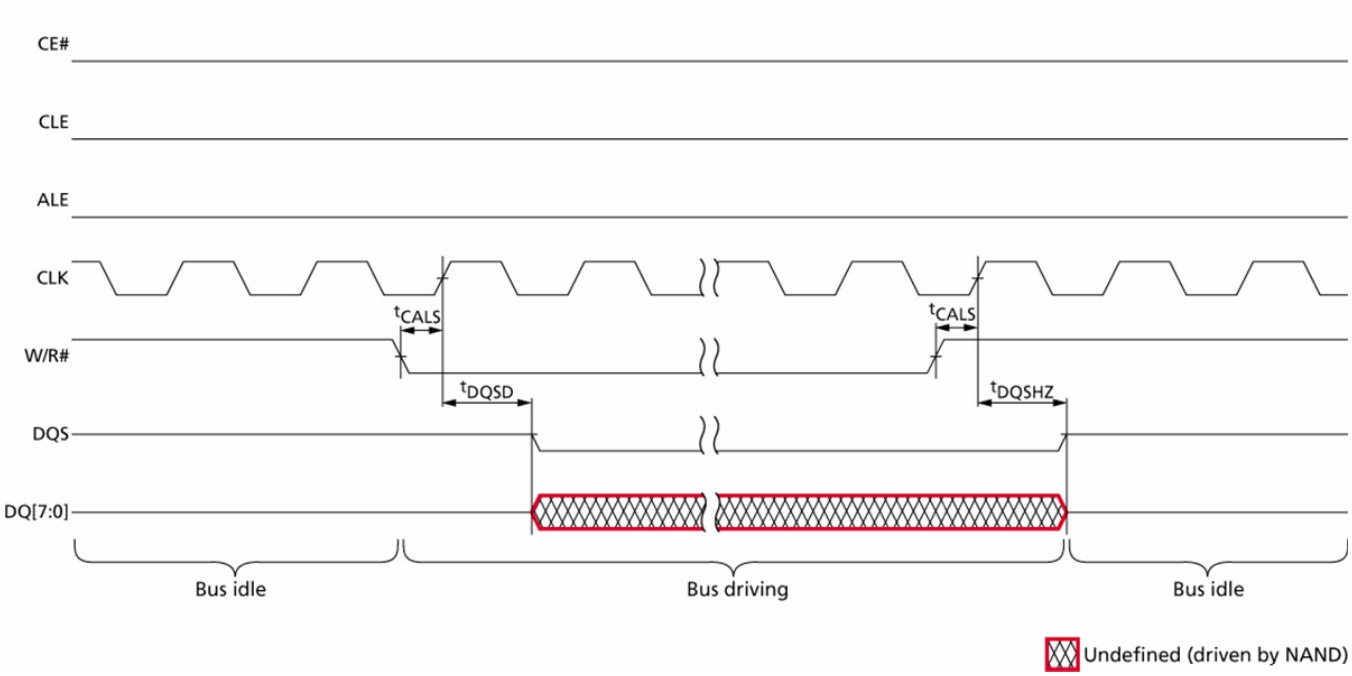
- CLK is running,
- CE# is LOW,
- ALE is LOW, and
- CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During Bus Idle all of the signals are enabled. DQS and DQ[7:0] are inputs. No commands, addresses, and data are latched into the target; no data is output. When entering Bus Idle the host must wait a minimum of tCAD before changing the bus mode. The only valid bus modes that are acceptable from Bus Idle are Bus Driving, Command, Address, and DDR Data Input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During bus driving all of the signals are enabled. DQS is LOW and DQ[7:0] is driven LOW or

HIGH, however no valid data is output. The only valid bus modes that are acceptable from Bus Driving are Bus Idle and DDR Data Output.

Figure 19: Bus Idle / Driving Behavior



1. Only the selected LUN drives DQS and DQ[7:0]. During a multi-LUN operation, the host must use the SELECT LUN WITH STATUS (78h) to prevent data output contention.

Synchronous Commands

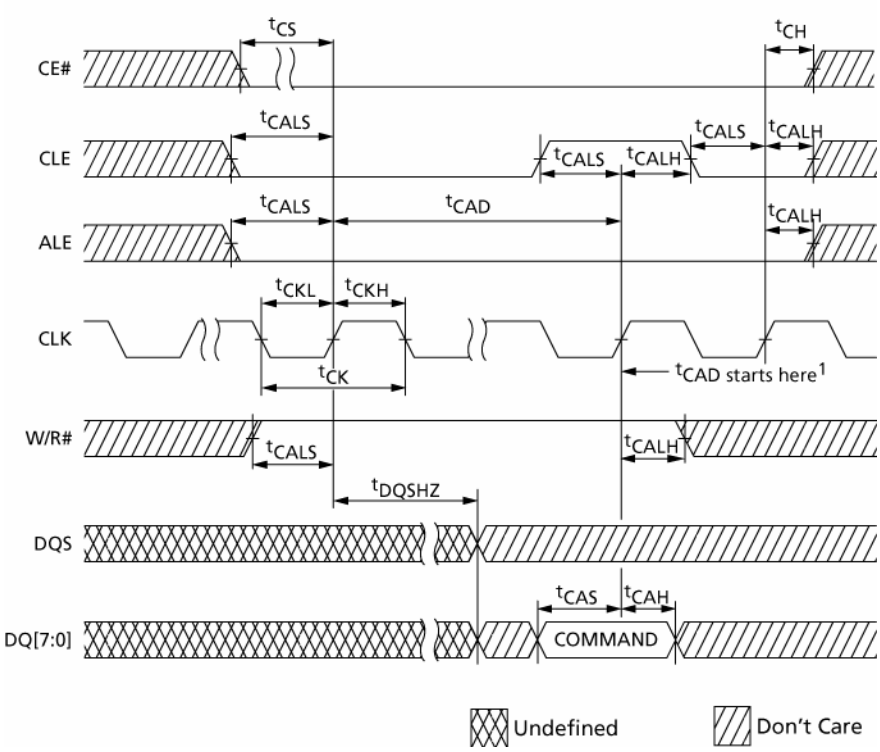
A command is written from DQ[7:0] to the command register on the rising edge of CLK when:

- CE# is LOW,
- ALE is LOW,
- CLE is HIGH, and
- W/R# is HIGH.

After a command is latched and prior to the next command, address, or data I/O mode, the bus must go to bus idle on the next rising edge of CLK except when the clock period, tCK, is greater than tCAD.

Commands are typically ignored by LUNs that are busy; however, some commands are accepted by LUNs even when they are busy, like READ STATUS (70h) and SELECT LUN WITH STATUS (78h).

Figure 20: Command Cycle



1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Synchronous Addresses

An address is written from DQ[7:0] to the address register on the rising edge of CLK when:

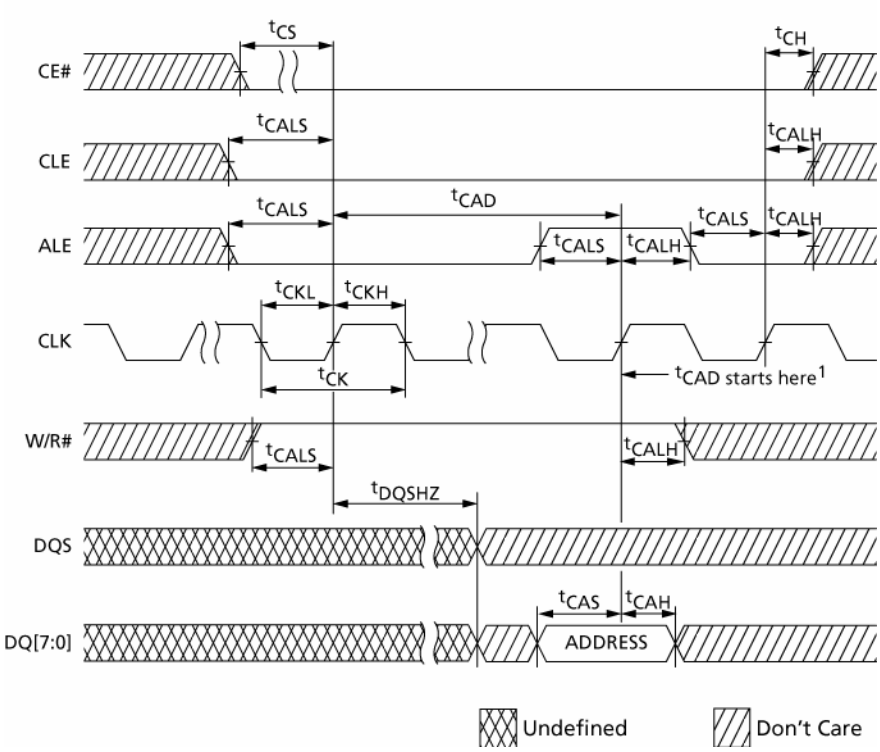
- CE# is LOW,
- ALE is HIGH,
- CLE is LOW, and
- W/R# is HIGH.

After an address is latched and prior to the next command, address, or data I/O mode, the bus must go to bus idle on the next rising edge of CLK except when the clock period, tCK, is greater than tCAD.

Bits not part of the address space must be LOW (see Table 2 on page 15). The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Table 5 on page 34).

Addresses are typically ignored by LUNs that are busy; however, some addresses are accepted by LUNs even when they are busy, like address cycles that follow the SELECT LUN WITH STATUS (78h) command.

Figure 21: Address Cycle



1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Synchronous DDR Data Input

To enter the DDR Data Input mode the following conditions must be met:

- CLK is running,
- CE# is LOW,
- W/R# is HIGH,
- tCAD is met,
- DQS is LOW, and
- ALE and CLE are HIGH on the rising edge of CLK.

Upon entering the DDR Data Input mode and after tDQSS, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when:

- CLK is running and DQS-to-CLK skew meets tDSH and tDSS,
- CE# is LOW,
- W/R# is HIGH, and
- ALE and CLE are HIGH on the rising edge of CLK.

To exit DDR Data Input mode the following conditions must be met:

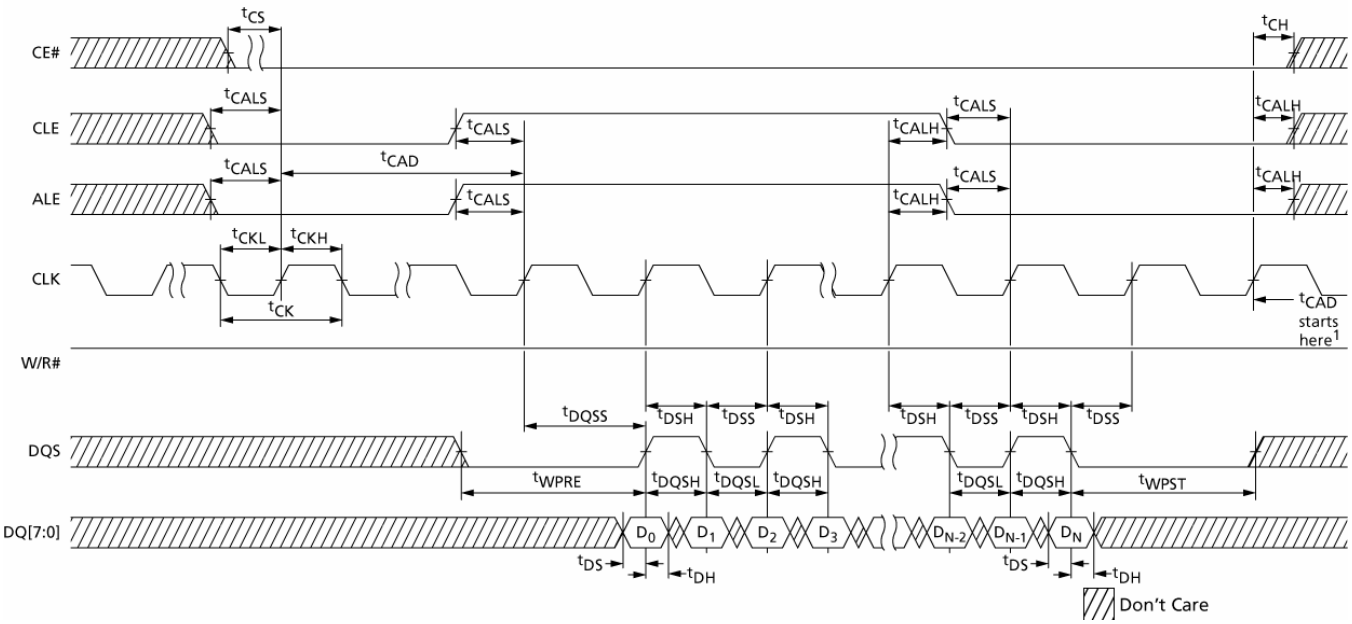
- CLK is running and DQS-to-CLK skew meets tDSH and tDSS,
- CE# is LOW,
- W/R# is HIGH,

- ALE and CLE are latched LOW on the rising edge of CLK,
- Data is written from DQ[7:0] to the cache register on the final rising and falling edges of DQS, and
- After the final falling edge of DQS, it is held low for tWPST.

After tWPST, the bus enters bus idle mode and tCAD begins on the next rising edge of CLK. Once tCAD starts the host can disable the target, if desired.

Data input is ignored by LUNs that are not selected or are busy.

Figure 22: DDR Data Input Cycles



1. When CE# remains LOW, tCAD begins at the first rising edge of the clock after tWPST completes.
2. tDSH (MIN) generally occurs during tDQSS (MIN).
3. tDSS (MIN) generally occurs during tDQSS (MAX).

Synchronous DDR Data Output

Data can be output from a LUN if it is ready. Data output is permitted following a READ operation from the NAND Flash array.

To enter the DDR Data Output mode the following conditions must be met:

- CLK is running,
- CE# is LOW,
- The host has released the DQ[7:0] bus and DQS,
- W/R# is latched LOW on the rising edge of CLK to allow the selected LUN to take ownership of the DQ[7:0] bus and DQS within tWRCK,
- tCAD is met, and
- ALE and CLE are HIGH on the rising edge of CLK.

Upon entering the DDR Data Output mode and DQS will toggle HIGH and LOW with a delay of tDQSCK from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than tAC.

DDR Data Output continues as long as:

- CLK is running,
- CE# is LOW,
- W/R# is LOW, and
- ALE and CLE are HIGH on the rising edge of CLK.

To exit DDR Data Output mode the following conditions must be met:

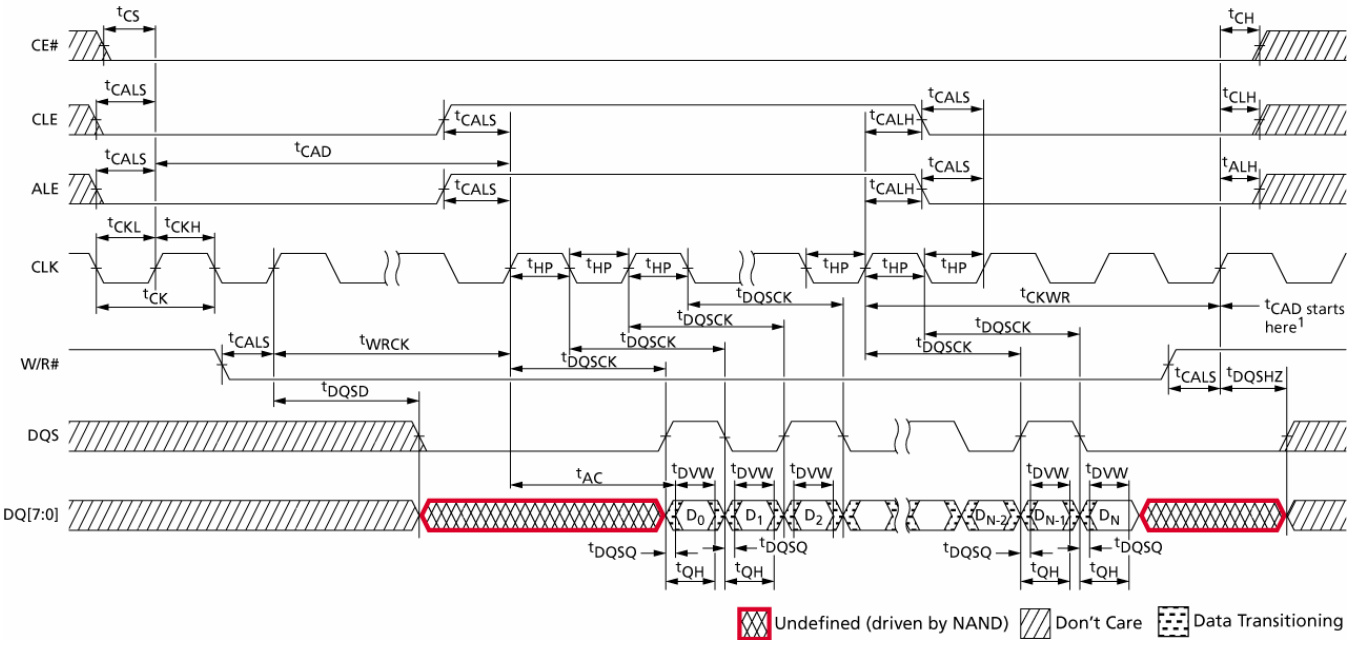
- CLK is running,
- CE# is LOW,
- W/R# is LOW, and
- ALE and CLE are latched LOW on the rising edge of CLK.

The final two data bytes will be output on DQ[7:0] on the final rising and falling edges of DQS after tDQSCK. After tCKWR, the bus enters bus idle mode and tCAD begins on the next rising edge of CLK. Once tCAD starts the host can disable the target if desired.

To prevent data contention following a Multi-LUN operation, the host must enable only one LUN for data output (see "Multi-LUN Operations" on page 72). Use the SELECT LUN WITH STATUS (78h) command to select the LUN that is to output data. Then issue the READ MODE (00h) command. Data can now be output from the selected LUN.

Data output requests are typically ignored by a LUN that is busy; however, it is permissible to output data from the status register even when a LUN is busy by first issuing the READ STATUS or SELECT LUN WITH STATUS (78h) command.

Figure 23: DDR Data Output Cycles



1. When CE# remains LOW, tCAD begins at the rising edge of the clock after tCKWR for subsequent command or data output cycle(s).
2. See Figure 19 on page 25 for details of W/R# behavior.
3. tAC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH: DQ[7:0] and DQS go to tri-state.

5. For W/R# transitioning LOW: DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See "Write Protect" under the "Asynchronous Interface" section on page 20.

Ready/Busy#

See "Ready/Busy#" under the "Asynchronous Interface" section on page 21.

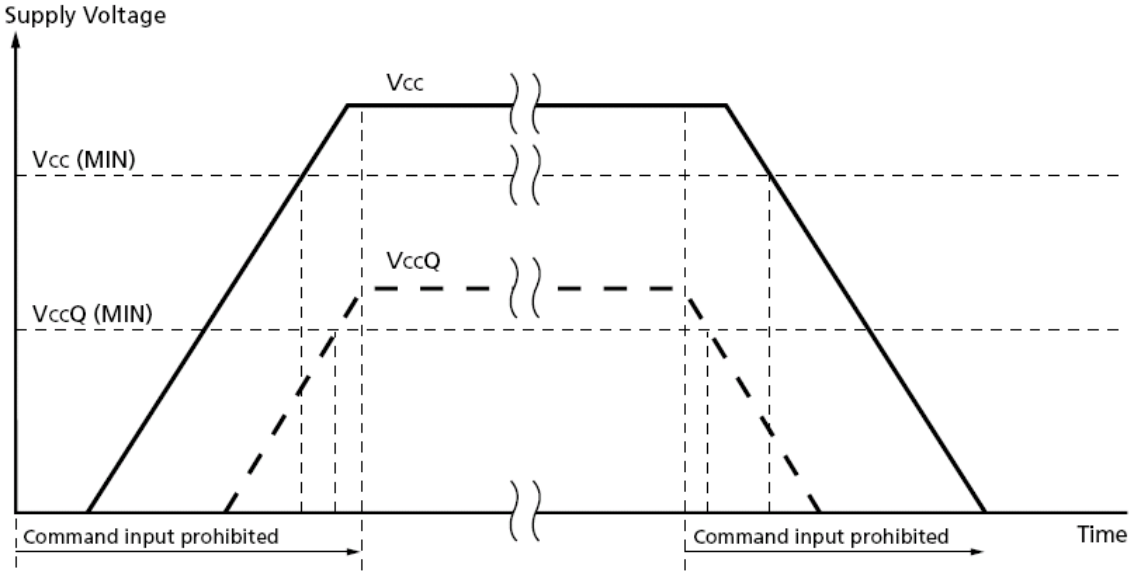
Vcc Power Cycling

These NAND Flash devices are designed to prevent data corruption during power transitions. Vcc is internally monitored. (The WP# signal permits additional hardware protection during power transitions.) When ramping Vcc and VccQ, use the following procedure to initialize the device:

1. Ramp Vcc to 2.7-3.6V.
2. Ramp VccQ to 1.7-1.95V not sooner than the Vcc ramp. VccQ must not exceed Vcc.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. See Figure 25 on page 31. The R/B# signal becomes valid when:
   a. 50µs has elapsed since the beginning the Vcc ramp, and
   b. 10µs has elapsed since VccQ reaches 1.7V.
4. If not monitoring R/B# the host must wait at least 100µs from VccQ reaching 1.7V.
5. All of the targets on the device power-on with the asynchronous interface active. Each NAND LUN draws less than an average of 10mA (IST) measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for a maximum of 1ms after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
7. The device is now initialized and ready for normal operation.

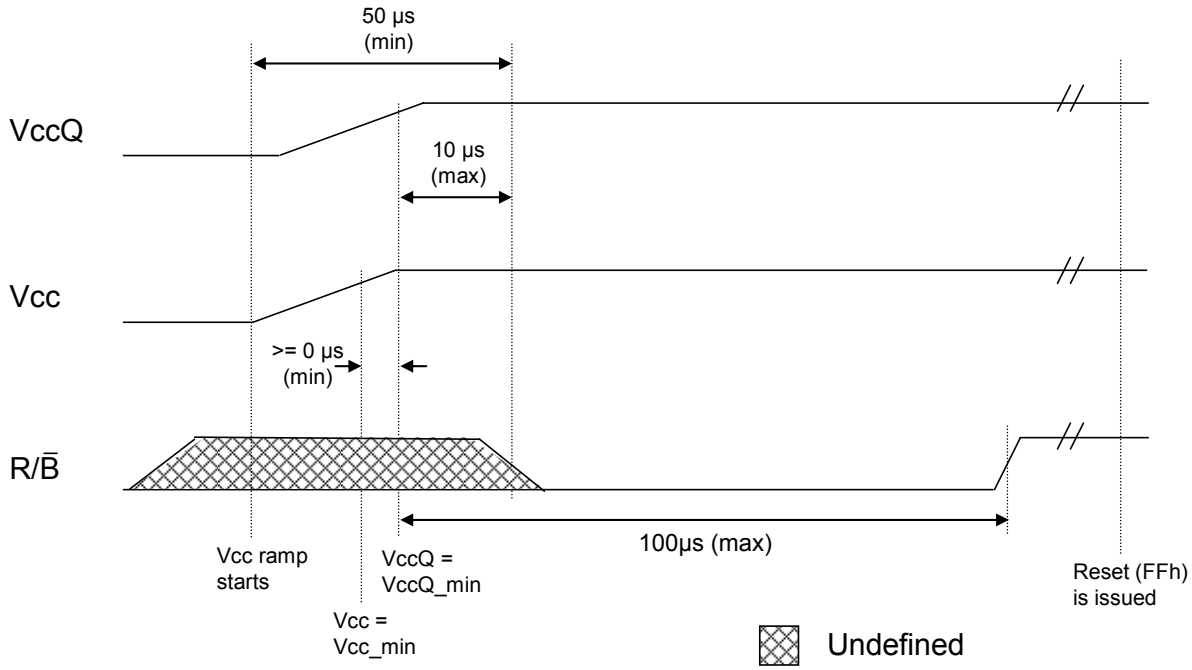
At power-down, VccQ must go LOW before or simultaneously with Vcc going LOW.

Figure 24: Power Cycle



1. Vcc is exaggerated over VccQ in this figure for illustrative purposes.

Figure 25: R/B# Power-on Behavior



Activating Interfaces

After performing the steps in the "VCC Power Cycling," the asynchronous interface is active for all targets on the device.

Each target's interface is independent of other targets, so the host is responsible to change the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface then the follow the procedure outlined in "Activating the Asynchronous Interface" below to resynchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command using an asynchronous command cycle.
3. R/B# goes LOW for tRST.
4. During tRST, but after tITC, the device enters the asynchronous NAND interface. READ STATUS (70h) and SELECT LUN WITH STATUS (78h) are the only commands that may be issued after tITC during tRST.
5. After tRST, R/B# goes HIGH. TIMING MODE feature address (01h), sub-feature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

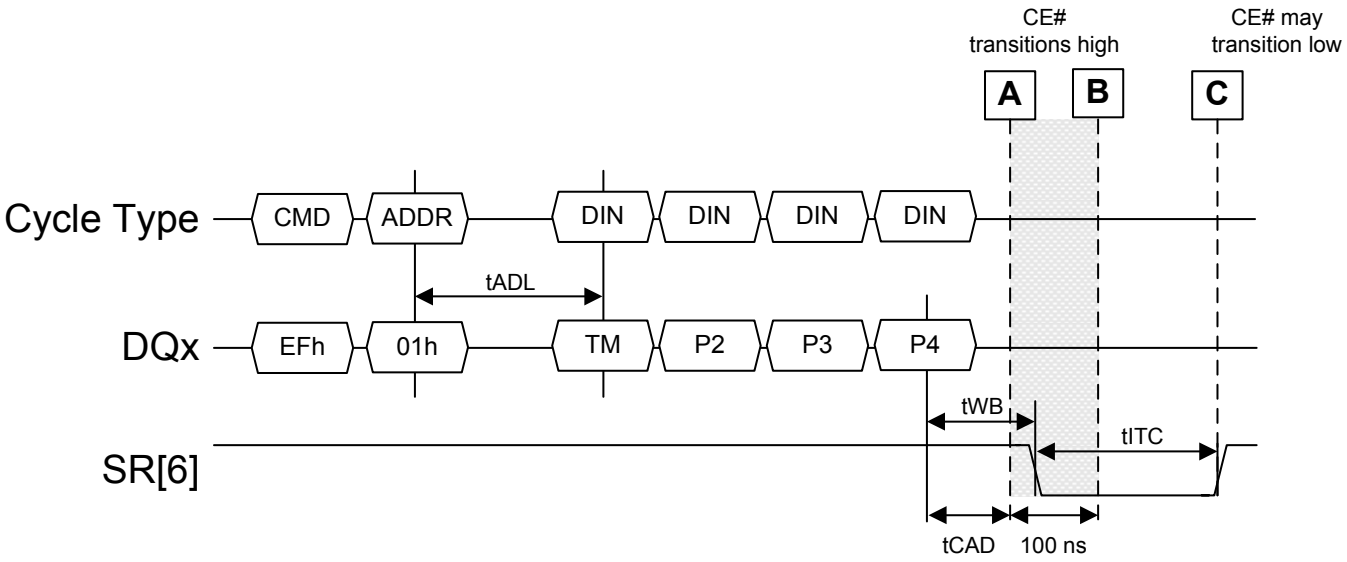
For further details, see "RESET FFh" on page 36.

Activating the Synchronous Interface

To activate the synchronous NAND interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the TIMING MODE.
3. Write P1 with 1Xh where "X" is the timing mode used in the synchronous interface (see Table 10 on page 46).
4. Write P2-P4 as 00h-00h-00h.
5. R/B# goes LOW for tITC. The host should pull CE# HIGH. During tITC the host should not issue any type of command, including status commands, to the NAND device.
6. After tITC, R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Figure 26: Activating the Synchronous Interface



1. TM = Timing Mode

Command Definitions

Table 5: Command Set

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid while Selected LUN Is Busy[1]	Valid while Other LUNs Are Busy[2]	Notes
Reset Operations							
RESET	FFh	0	—	—	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	—	—	Yes	Yes	
Identification Operations							
READ ID	90h	1	—	—			3
READ PARAMETER PAGE	ECh	1	—	—			
READ UNIQUE ID	EDh	1	—	—			
Configuration Operations							
GET FEATURES	EEh	1	—	—			3
SET FEATURES	EFh	1	4	—			4
Status Operations							
READ STATUS	70h	0	—	—	Yes		
SELECT LUN WITH STATUS	78h	3	—	—	Yes	Yes	
Column Address Operations							
CHANGE READ COLUMN	05h	2	—	E0h		Yes	
SELECT CACHE REGISTER	06h	5	—	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	—		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	—		Yes	
Read Operations							
READ MODE	00h	0	—	—		Yes	
READ PAGE	00h	5	—	30h		Yes	5
READ PAGE MULTI-PLANE	00h	5	—	32h		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	—	—		Yes	6
READ PAGE CACHE RANDOM	00h	5	—	31h		Yes	5, 6
READ PAGE CACHE LAST	3Fh	0	—	—		Yes	6
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h		Yes	
PROGRAM PAGE MULTI-PLANE	80h	5	Yes	11h		Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h		Yes	7
Erase Operations							
ERASE BLOCK	60h	3	—	D0h		Yes	
ERASE BLOCK MULTI-PLANE	60h	3	—	D1h		Yes	
Copyback Operations							
COPYBACK READ	00h	5	—	35h		Yes	5
COPYBACK PROGRAM	85h	5	Optional	10h		Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h		Yes	

1. Busy means RDY = "0".
2. These commands may be used for Multi-LUN operations. See page 71.

3. The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
5. This command can be preceded by the READ PAGE MULTI-PLANE (00h-32h) command up to three times, to permit the maximum of a simultaneous four-plane array operation.
6. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = "1", ARDY = "0") is permissible if the previous command is a READ PAGE (00h-30h) or READ PAGE CACHE-series command, otherwise it is prohibited.
7. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = "1", ARDY = "0") is permissible if the previous command is a PROGRAM PAGE CACHE (80h-15h) command, otherwise it is prohibited.

Reset Operations

RESET FFh

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all LUNs, even when they are busy.

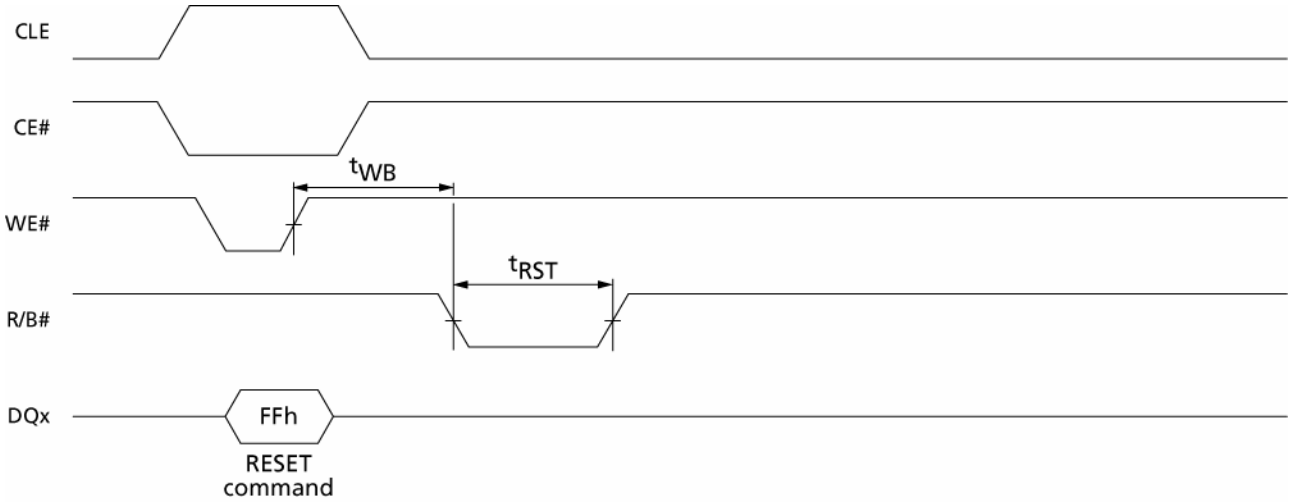
When FFh is written to the command register, the target goes busy for tRST. During tRST the selected target (CE#) discontinues all array operations on all LUNs. All pending single-plane and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more LUNs, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

If the RESET (FFh) command is issued when the synchronous interface is enabled, the target's interface is changed to the asynchronous interface and the timing mode is set to timing mode 0. The RESET (FFh) command may be issued asynchronously when the synchronous interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched the host should not issue any commands during tITC. After tITC, but during or after tRST, the host may poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after tRST, the host may poll each LUN's status register.

This command must be issued as the first command to each target after power-up. See "VCC Power Cycling" on page 30. Use of the SELECT LUN WITH STATUS (78h) command is prohibited during the power-on RESET. Instead, READ STATUS (70h) can be used to determine when the target is ready.

Figure 27: RESET (FFh) Cycle



SYNCHRONOUS RESET FCh

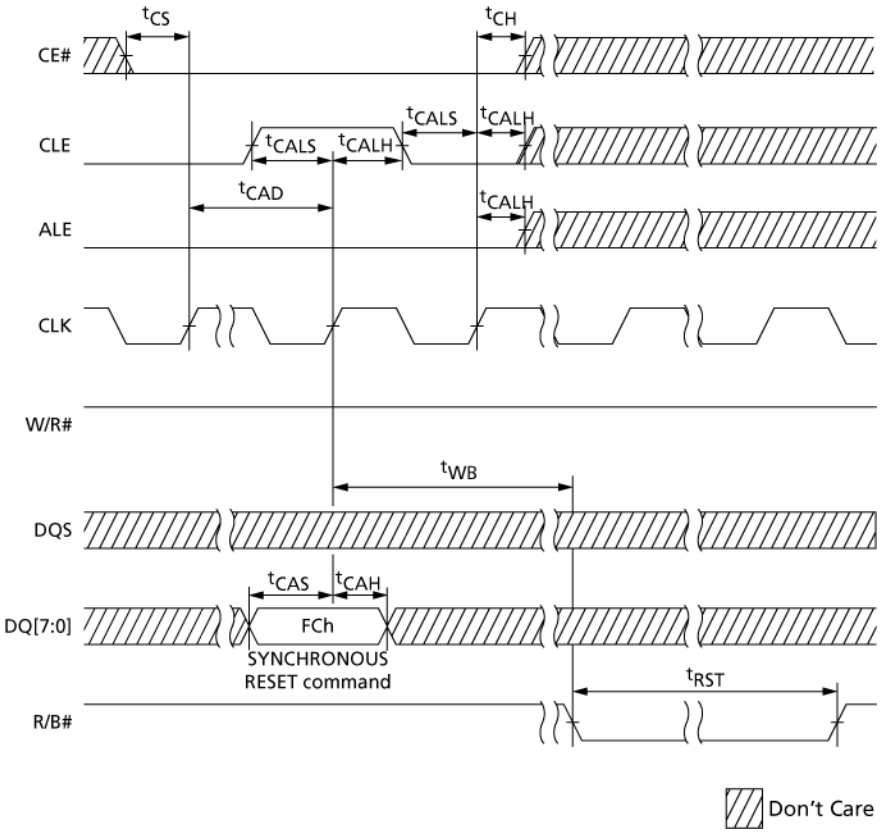
The SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort a command sequence in progress when the synchronous interface is active. This command is accepted by all LUNs, even when they are BUSY.

When FCh is written to the command register, the target goes busy for tRST. During tRST the selected target (CE#) discontinues all array operations on all LUNs. All pending single-plane and multi-plane operations are cancelled. The cache register contents are no longer valid. The synchronous interface remains active.

During or after tRST, the host may poll each LUN's status register.

This command is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.

Figure 28: SYNCHRONOUS RESET (FCh) Cycle



Identification Operations

READ ID 90h

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all LUNs on the target are idle.

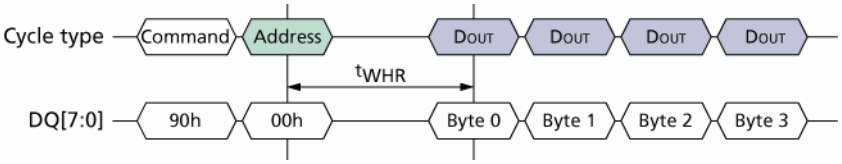
Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by an address cycle of 00h, the target returns a 5-byte identifier code that includes the manufacturer's ID, device configuration, and part-specific information.

When the 90h command is followed by an address cycle of 20h, the target returns the 4-byte ONFI identifier code.

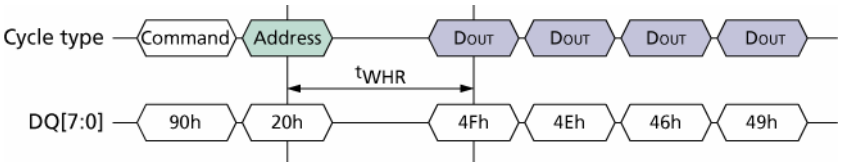
After the 90h and address cycle are written to the target the host enables data output mode to read the identifier information. When the asynchronous interface is active one data byte comes out per RE# toggle. When the synchronous interface is active, one data byte comes out per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 29: READ ID (90h) with 00h Address Cycle Operation



1. See Table 6 for byte definitions.

Figure 30: READ ID (90h) with 20h Address Cycle Operation



1. See Table 7 for byte definitions.

Table 6: Read ID Parameters for Address 00h

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Byte 0 – Manufacturer ID											
Manufacturer	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1 – Device ID											
MT29H8G08A	8Gb Vcc=3.3V	0	0	1	1	1	0	0	0	38h	
MT29H16G08E	16Gb Vcc=3.3V	0	0	1	1	1	0	0	0	38h	2
MT29H32G08G	32Gb Vcc=3.3V	0	1	0	0	1	0	0	0	48h	3
Byte 2											
LUNs per CE#	1							0	0	00b	
	2							0	1	01b	
Cell type	SLC					0	0			00b	
Reserved		0	0	0	0					0000b	
8Gb SDP		0	0	0	0	0	0	0	0	00h	
16Gb DDP		0	0	0	0	0	0	0	0	00h	
32Gb QDP		0	0	0	0	0	0	0	1	01h	
Byte 3											
Page size	4KB							1	0	10b	
Spare area size per 512B	28B					0	1			01b	
Pages per block	128		0	1	0					010b	
Multi-LUN operations	Not supported	0								0b	
	Supported	1								1b	
8Gb SDP		0	0	1	0	0	1	1	0	26h	
16Gb DDP		0	0	1	0	0	1	1	0	26h	
32Gb QDP		1	0	1	0	0	1	1	0	A6h	
Byte 4											
Planes per LUN	4							1	0	10b	
Blocks per LUN	2,048				0	0	1			001b	
Timing Mode: Asynchronous	4 (25ns)	1	0	0						100b	
8Gb SDP		1	0	0	0	0	1	1	0	86h	
16Gb DDP		1	0	0	0	0	1	1	0	86h	
32Gb QDP		1	0	0	0	0	1	1	0	86h	

1. b = binary, h = hexadecimal
2. The device code reflects the configuration of each 8Gb target.
3. The device code reflects the configuration of each 16Gb target.

Table 7: Read ID Parameters for Address 20h

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Byte 0	"O"	0	1	0	0	1	1	1	1	4Fh	
Byte 1	"N"	0	1	0	0	1	1	1	0	4Eh	
Byte 2	"F"	0	1	0	0	0	1	1	0	46h	
Byte 3	"I"	0	1	0	0	1	0	0	1	49h	
Byte 4	Undefined	X	X	X	X	X	X	X	X	XXh	

1. h = hexadecimal

READ PARAMETER PAGE ECh

The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all LUNs on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an address cycle of 00h, the target goes busy for tR. If the READ STATUS (70h) command is used to monitor for command completion the READ MODE (00h) command must be used to re-enable data output mode. Use of the SELECT LUN WITH STATUS (78h) command is prohibited while the target is busy and during data output.

After tR completes the host enables data output mode to read the parameter page. When the asynchronous interface is active one data byte comes out per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte per rising or falling edge of DQS.

A minimum of seven copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the SELECT CACHE REGISTER (06h-E0h) is prohibited.

Figure 31: READ PARAMETER PAGE (ECh) Operation

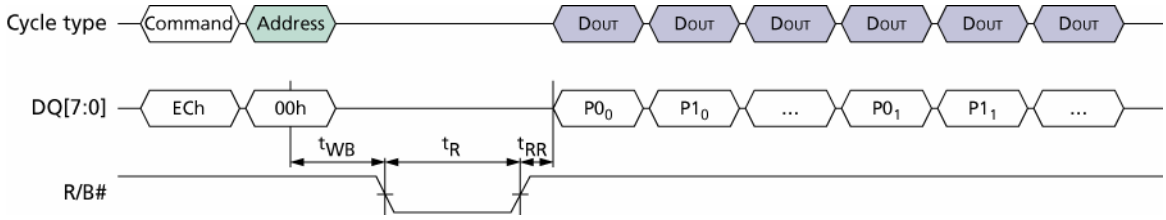


Table 8: Parameter Page Definition

Byte	Description	Device	Values
Revision information and features block			
0-3	Parameter page signature Byte 0: "O" Byte 1: "N" Byte 2: "F" Byte 3: "I"	—	4Fh, 4Eh, 46h, 49h
4-5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports ONFI 2.0 Bit 1: 1 = supports ONFI 1.0 Bit 0: Reserved (0)	—	06h, 00h
6-7	Features supported Bit[15:6]: Reserved (0) Bit 5: 1 = supports synchronous interface Bit 4: 1 = supports odd to even page copyback Bit 3: 1 = supports interleaved (multi-plane) operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29H8G08ACA	38h, 00h
		MT29H16G08ECA	38h, 00h
		MT29H32G08GCA	3Ah, 00h

Byte	Description	Device	Values
8-9	Optional commands supported Bit[15:6]: Reserved (0) Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports SELECT LUN WITH STATUS Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports READ CACHE SEQUENTIAL Bit 0: 1 = supports PROGRAM PAGE CACHE	—	3Fh, 00h
10-31	Reserved (0)	—	All 00h
Manufacturer information block			
32-43	Device manufacturer (12 ASCII characters) "MICRON "	—	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII characters)	MT29H8G08ACA	4Dh, 54h, 32h, 39h, 48h, 38h, 47h, 30h, 38h, 41h, 43h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29H16G08ECA	4Dh, 54h, 32h, 39h, 48h, 31h, 36h, 47h, 30h, 38h, 45h, 43h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29H32G08GCA	4Dh, 54h, 32h, 39h, 48h, 33h, 32h, 47h, 30h, 38h, 47h, 43h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	—	2Ch
65-66	Date code (not supported)	—	00, 00h
67-79	Reserved (0)	—	All 00h
Memory organization block			
80-83	Number of data bytes per page	—	00h, 10h, 00h, 00h
84-85	Number of spare bytes per page	—	E0h, 00h
86-89	Number of data bytes per partial page	—	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	—	1Ch, 00h
92-95	Number of pages per block	—	80h, 00h, 00h, 00h
96-99	Number of blocks per LUN	—	00h, 08h, 00h, 00h
100	Number of LUNs	MT29H8G08ACA	01h
		MT29H16G08ECA	01h
		MT29H32G08GCA	02h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	—	23h
102	Number of bits per cell	—	01h
103-104	Bad blocks maximum per LUN	—	32h, 00h
105-106	Block endurance	—	01h, 05h
107	Guaranteed valid blocks at beginning of target	—	01h
108-109	Block endurance for guaranteed valid blocks	—	00h, 00h
110	Number of programs per page	—	02h

Byte	Description	Device	Values
111	Partial programming attributes Bit[7:5]: Reserved (0) Bit 4: 1 = partial page layout is partial page data followed by partial page spare Bit[3:1]: Reserved (0) Bit 0: 1 = partial page programming has constraints	—	00h
112	Number of bits ECC correctability	—	08h
113	Number of interleaved (multi-plane) address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	—	02h
114	Interleaved (multi-plane) operation attributes Bit[7:4]: Reserved (0) Bit 3: Address restrictions for program cache Bit 2: 1 = program cache supported Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	—	0Eh
115-127	Reserved (0)	—	All 00h
Electrical parameters block			
128	I/O pin capacitance, maximum	MT29H8G08ACA	05h
		MT29H16G08ECA	05h
		MT29H32G08GCA	0Ah
129-130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: supports timing mode 5 Bit 4: supports timing mode 4 Bit 3: supports timing mode 3 Bit 2: supports timing mode 2 Bit 1: supports timing mode 1 Bit 0: supports timing mode 0	—	1Fh, 00h
131-132	Asynchronous program cache timing mode support Bit[15:6]: Reserved (0) Bit 5: supports timing mode 5 Bit 4: supports timing mode 4 Bit 3: supports timing mode 3 Bit 2: supports timing mode 2 Bit 1: supports timing mode 1 Bit 0: supports timing mode 0	—	1Fh, 00h
133-134	tPROG maximum page programming time (µs)	—	F4h, 01h
135-136	tBERS maximum block erase time (µs)	—	10h, 27h
137-138	tR maximum page read time (µs)	—	19h, 00h
139-140	tCCS minimum change column setup time (ns)	—	C8h, 00h
141-142	Source synchronous timing mode support Bit[15:4]: Reserved (0) Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	—	1Fh, 00h
143	Source synchronous features Bit[7:2]: Reserved (0) Bit 1: 1 = typical capacitance values present Bit 0: 0 = tCAD is 25ns	—	02h
144-145	CLK input pin capacitance, typical	MT29H8G08ACA	25h, 00h
		MT29H16G08ECA	25h, 00h

Byte	Description	Device	Values
		MT29H32G08GCA	42h, 00h
146-147	I/O pin capacitance, typical	MT29H8G08ACA	2Ch, 00h
		MT29H16G08ECA	2Ch, 00h
		MT29H32G08GCA	4Dh, 00h
148-149	Input pin capacitance, typical	MT29H8G08ACA	28h, 00h
		MT29H16G08ECA	28h, 00h
		MT29H32G08GCA	44h, 00h
150	Input capacitance, maximum	MT29H8G08ACA	05h
		MT29H16G08ECA	05h
		MT29H32G08GCA	0Ah
151	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = supports Overdrive 2 drive strength Bit 1: 1 = supports Overdrive 1 drive strength Bit 0: 1 = supports driver strength settings	—	07h
152-163	Reserved (0)	—	All 00h
Vendor block			
164-165	Vendor-specific revision number	—	01h, 00h
166	Multi-plane page read support Bit[7:1]: Reserved (0) Bit 0: 1 = supports multi-plane page read	—	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 1 = supports Micron-specific read cache	—	00h
168	Read Unique ID support Bit[7:1]: Reserved (0) Bit 0: 1 = supports Micron-specific	—	00h
169	Programmable I/O drive strength support Bit[7:1]: Reserved (0) Bit 0: 1 = supports B8h command	—	00h
170	Number of programmable I/O drive strength settings Bit[7:3]: Reserved (0) Bit[2:0]: Number of drive strength settings	—	04h
171	Programmable I/O drive strength feature address	—	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = supports programmable I/O drive strength	—	01h
173	Programmable R/B# pull-down strength feature address	—	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0]: Number of R/B# pull-down strength settings	—	04h
175	OTP support Bit[7:2]: Reserved (0) Bit 1: 1 = supports Get/Set Features command set Bit 0: 1 = supports A5h/A0h/AFh OTP command set	—	02h
176	OTP page address start	—	02h
177	OTP protect page address	—	01h
178	Number of OTP pages	—	0Ah
179	OTP feature address	—	90h
180-253	Reserved (0)	—	All 00h
254-255	Integrity CRC	MT29H8G08ACA	F1h, 75h
		MT29H16G08ECA	9Fh, B5h

Byte	Description	Device	Values
		MT29H32G08GCA	48h, 81h
Redundant Parameter Pages			
256-511	Parameter page copy #2	—	See bytes 0-255
512-767	Parameter page copy #3	—	See bytes 0-255
768-1023	Parameter page copy #4	—	See bytes 0-255
1024-1279	Parameter page copy #5	—	See bytes 0-255
1280-1535	Parameter page copy #6	—	See bytes 0-255
1536-1791	Parameter page copy #7	—	See bytes 0-255
1792-4319	Reserved (FFh)	—	All FFh

READ UNIQUE ID EDh

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all LUNs on the target are idle.

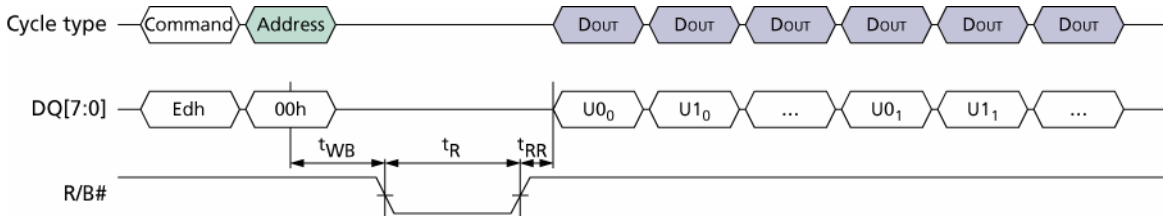
Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When the EDh command is followed by an address cycle of 00h, the target goes busy for tR. If the READ STATUS (70h) command is used to monitor for command completion the READ MODE (00h) command must be used to re-enable data output mode.

After tR completes the host enables data output mode to read the unique ID. When the asynchronous interface is active one data byte comes out per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte per rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. Of these 32 bytes, the first 16 bytes are unique data and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh then that copy of the unique ID data is correct. In the event that there is non-FFh result, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command may be used to change the location of data output. Use of the SELECT CACHE REGISTER (06h-E0h) command is prohibited.

Figure 32: READ UNIQUE ID (EDh) Operation



Configuration Operations

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which sub-feature parameters are to be read or modified. Each feature address (in the range of 00h to FFh) is defined in Table 9. The GET FEATURES command reads the sub-feature parameters (P1–P4) at the specified feature address. The SET FEATURES (EFh) command writes sub-feature parameters (P1–P4) to the specified feature address.

Table 9: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h-0Fh	Reserved
10h	Programmable output drive strength
11h-7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable R/B# pull-down strength
82h-8Fh	Reserved
90h	Array operation mode
91h-FFh	Reserved

SET FEATURES EFh

The SET FEATURES (EFh) command writes the sub-feature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all LUNs on the target are idle.

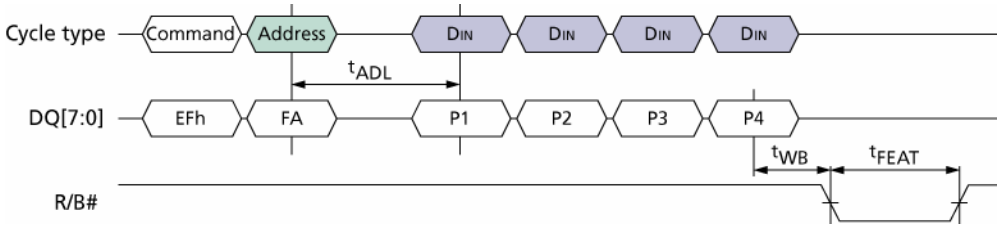
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address as specified in Table 9. The host waits for tADL before the sub-feature parameters are input. When the asynchronous interface is active one sub-feature parameter is latched per rising edge of WE#. When the synchronous interface is active, one sub-feature parameter is latched per rising edge of DQS; the data on the falling edge of DQS should be identical to the sub-feature parameter input on the previous rising edge of DQS.

After all four sub-feature parameters are input, the target goes busy for tFEAT. The READ STATUS (70h) command may be used to monitor for command completion.

Feature address 01h (Timing Mode) is unique from the other feature addresses. If SET FEATURES is used to modify the Interface Type then the target will be busy for tITC. See "Activating Interfaces" on page 32 for more details.

Figure 33: SET FEATURES (EFh) Operation



GET FEATURES EEh

The GET FEATURES (EEh) command reads the sub-feature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all LUNs on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for tFEAT. If the READ STATUS (70h) command is used to monitor for command completion the READ MODE (00h) command must be used to re-enable data output mode. Use of the SELECT LUN WITH STATUS (78h) command is prohibited prior to and during data output.

After tFEAT completes, the host enables data output mode to read the sub-feature parameters. When the asynchronous interface is active one data byte comes out per RE# toggle. When the synchronous interface is active, one data byte comes out per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 34: GET FEATURES (EEh) Operation

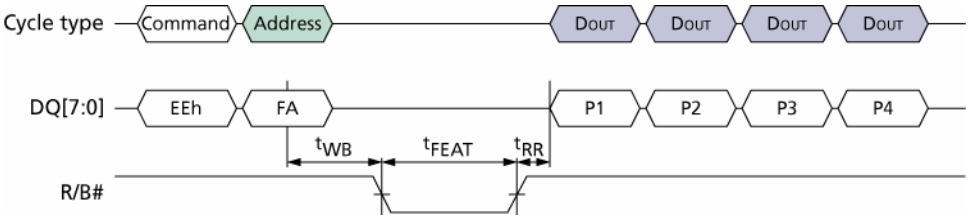


Table 10: Feature Address 01h: Timing Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing Mode	Mode 0 (default)					0	0	0	0	x0h	1
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
Data Interface	Asynchronous (default)			0	0					0xh	
	Synchronous DDR			0	1					1xh	
	Reserved			1	x					2xh	
Reserved		0	0							00b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

1. Asynchronous timing mode 0 is the default, power-on value.

Table 11: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output Drive Strength	Overdrive 2							0	0	00h	1
	Overdrive 1							0	1	01h	
	Nominal (default)							1	0	02h	
	Underdrive							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

1. See "Output Drive Strength" on page 74 for more details.

Table 12: Feature Address 81h: Programmable R/B# Pull-down Strength

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# Pull-down Strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 13: Feature Address 90h: Array Operation Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

1. See "One-Time Programmable (OTP) Operations" on page 68 for more details.

Status Operations

Each LUN provides its status independently of other LUNs on the same target through its 8-bit status register.

Once the READ STATUS (70h) or SELECT LUN WITH STATUS (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the synchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles while ALE and CLE are HIGH.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (tR) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see READ MODE 00h on page 55).

The READ STATUS (70h) command returns the status of the most recently selected LUN. To prevent data contention during or following a Multi-LUN operation, the host must enable only one LUN for status output by using the SELECT LUN WITH STATUS (78h) command (see “Multi-LUN Operations” on page 72).

Table 14: Status Register Definition

SR Bit	Definition	Independent per Plane[1]	Description
7	WP#	—	Write Protect: "0" = Protected "1" = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to "0" if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	—	Ready/Busy I/O: "0" = Busy "1" = Ready This bit indicates that the selected LUN is not available to accept new commands, address, or data I/O cycles with the exception of RESET (FFh), SYNCHRONOUS RESET (FCh), READ STATUS (70h), and SELECT LUN WITH STATUS (70h). *This bit applies only to the selected LUN.*
5	ARDY	—	Ready/Busy Array: "0" = Busy "1" = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected LUN. It goes HIGH when all array operations on the selected LUN finish. *This bit applies only to the selected LUN.*
4	—	—	Reserved (0)
3	—	—	Reserved (0)
2	—	—	Reserved (0)
1	FAILC	Yes	Pass/Fail (N-1): "0" = Pass "1" = Fail This bit is set if the previous operation on the selected LUN failed. This bit is valid only with RDY (SR bit 6) is "1." It applies to Program- and Copyback Program-series operations (80h-10h, 80h-15h, 85h-10h). This bit is not valid following a READ-series operation.
0	FAIL	Yes	Pass/Fail (N): "0" = Pass "1" = Fail This bit is set if the most recently finished operation on the selected LUN failed. This bit is valid only when ARDY (SR bit 5) is "1." It applies to Program-, Erase-, and Copyback Program-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

1. After a multi-plane operation begins the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command is issued. Once the SELECT LUN WITH STATUS (78h) command is issued the FAILC and FAIL bits reflect the status of the plane selected.

READ STATUS 70h

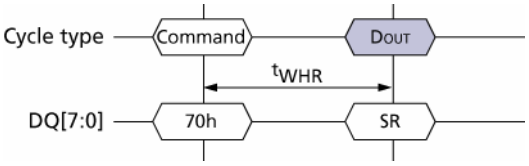
The READ STATUS (70h) command returns the status of the last selected LUN on a target. This command is accepted by the last selected LUN even when it is busy (RDY = "0").

If there is only one LUN per target then the READ STATUS (70h) command may be used following all NAND commands to return the status.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select the LUN that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more LUNs may respond until the next operation is issued. The READ STATUS (70h) command may be used following all single-LUN operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = "1"), use the SELECT LUN WITH STATUS (78h) command—once for each plane— to determine which plane operation failed.

Figure 35: READ STATUS (70h) Operation



SELECT LUN WITH STATUS 78h

The SELECT LUN WITH STATUS (78h) command returns the status of the addressed LUN on a target even when it is busy (RDY = "0"). This command is accepted by all LUNs, even when they are BUSY (RDY = "0").

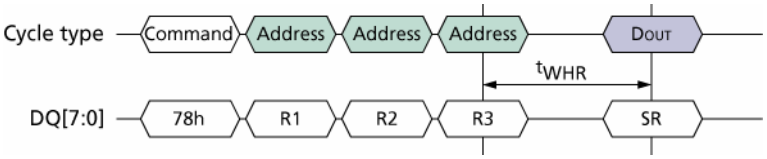
Writing 78h to the command register followed by three row address cycles containing the page, block, and LUN addresses puts the selected LUN into the status mode. The selected LUN stays in this mode until another valid command is issued. LUNs that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected LUN. The FAILC and FAIL bits are specific to the plane specified in the row address.

The SELECT LUN WITH STATUS (78h) command additionally enables the selected LUN for data output. To begin data output following a READ-series operation and after the selected LUN is ready (RDY = "1"), issue the READ MODE (00h) command and then begin data output. If the host needs to change which cache register will output data, use the SELECT CACHE REGISTER (06h-E0h) command after the LUN is ready (see page 51).

Use of the SELECT LUN WITH STATUS (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other Reset, Identification, and Configuration operations. See these operations for more specific details.

Figure 36: SELECT LUN WITH STATUS (78h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the LUNs of a target. These features provide flexibility to the

host in how to manage data, especially when the host's internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, the column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to "0") since data is transferred on DQ[7:0] in two-byte units.

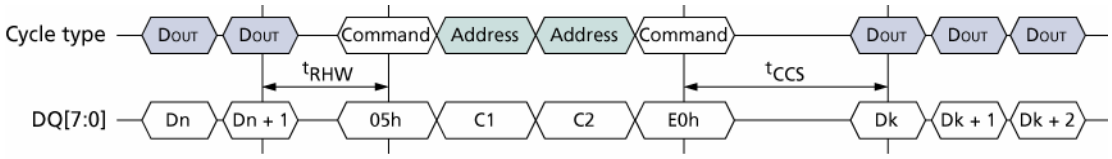
CHANGE READ COLUMN 05h-E0h

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output of the last selected LUN. This command is accepted by the selected LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the selected LUN during a cache read operation (RDY = "1" and ARDY = "0").

Writing 05h to the command register followed by two column address cycles containing the column address, followed by the E0h command puts the selected LUN into data output mode. After the E0h command cycle is issued the host must wait at least tCCS before requesting data output. The selected LUN stays in data output mode until another valid command is issued.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the SELECT LUN STATUS (78h) command will result in bus contention, as two or more LUNs may output data.

Figure 37: CHANGE READ COLUMN (05h-E0h) Operation



SELECT CACHE REGISTER 06h-E0h

The SELECT CACHE REGISTER (06h-E0h) command enables data output on the addressed LUN and cache register at the specified column address. This command is accepted by a LUN when it is ready (RDY = "1", ARDY = "1").

Writing 06h to the command register followed by two column address cycles and three row address cycles, followed by E0h enables data output mode on the address LUN and cache register at the specified column address. After the E0h command cycle is issued the host must wait at least tCCS before requesting data output. The selected LUN stays in data output mode until another valid command is issued.

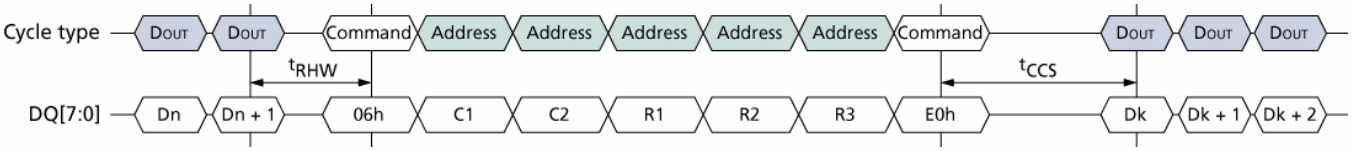
Following a multi-plane read page operation the SELECT CACHE REGISTER (06h-E0h) command is used to select which cache register is enabled for data output. After data output is complete on the selected plane it may be issued again to begin data output on another plane.

In devices with more than one LUN per target, the SELECT CACHE REGISTER (06h-E0h) command may be used following a multi-LUN read operation after all of the LUNs on the target are ready (RDY = "1"). LUNs that are not addressed are deselected to avoid bus contention.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command may be used instead.

Use of the SELECT CACHE REGISTER (06h-E0h) command is prohibited during and following READ PAGE CACHE-series (31h, 00h-31h) operations.

Figure 38: SELECT CACHE REGISTER (06h-E0h)



CHANGE WRITE COLUMN 85h

The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last selected LUN. This command is accepted by the selected LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the selected LUN during cache program operations (RDY = "1" and ARDY = "0").

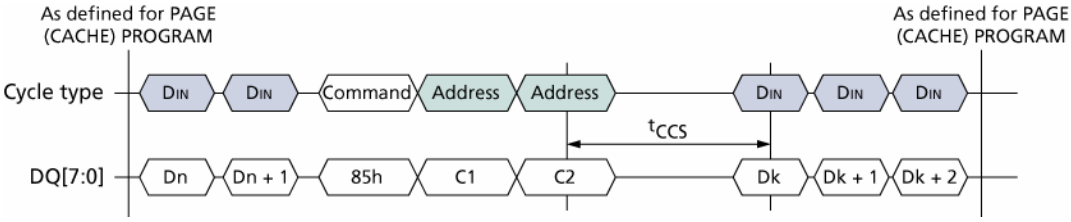
Writing 85h to the command register followed by two column address cycles containing the column address puts the selected LUN into data input mode. After the second address cycle is issued the host must wait at least tCCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

After COPYBACK READ (00h-35h) and READ PAGE (00h-30h) operations when data output is enabled, the CHANGE WRITE COLUMN (85h) command may be used to enable data input to modify cache register contents. To re-enable data output use the CHANGE READ COLUMN (05h-E0h) command. The use of these CHANGE READ COLUMN (05h-E0h) and CHANGE WRITE COLUMN (85h) sequences can be repeated multiple times. When finished reading and modifying the cache register the host can issue the COPYBACK PROGRAM (85h-10h) operation to program the cache register contents to its corresponding plane. This behavior allows data to be processed in the cache register in small sections to reduce the amount of buffer memory used in the host controller. See "Copyback Operations" on page 65 for more details.

In devices that have more than one LUN per target, the CHANGE WRITE COLUMN (85h) command is permitted with other commands that support multi-LUN operations.

Figure 39: CHANGE WRITE COLUMN (85h) Operation



CHANGE ROW ADDRESS 85h

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND array. It also changes the column address of the selected cache register and enables data input on the specified LUN. This command is accepted by the selected LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the selected LUN during cache program operations (RDY = "1" and ARDY = "0").

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least tCCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

This command allows the host to modify the page and block destination location for the data in the cache register from the originally specified page and block address. This is particularly useful for block management when data input does not end at the page boundary.

In devices that have more than one LUN per target, the CHANGE ROW ADDRESS (85h) command is permitted with other commands that support multi-LUN operations.

Read Operations

Read operations are used to copy data from the NAND array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE WRITE COLUMN (85h).

Multi-Plane Read Operations

Multi-Plane Read Page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the LUN is ready, the SELECT CACHE REGISTER (06h-E0h) command determines which plane outputs data. During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE WRITE COLUMN (85h).

See "Multi-Plane Operations" on page 71 for more details.

Read Cache Operations

For the highest sustainable level of data throughput, the Read Page Cache-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a Read Page Cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during tR and the selected LUN is busy (RDY = "0", ARDY = "0"). After tR (R/B# is HIGH and RDY = "1", ARDY = "1"), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) to begin copying the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h) to begin copying the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target and RDY = "0" and ARDY = "0" on the LUN for tRCBSY while the next page begins copying data from the array to the data register. After tRCBSY, R/B# goes HIGH and the LUN's status register bits indicate that the device is busy with a cache operation (RDY = "1", ARDY = "0"). The cache register is now available and the page requested in the read page cache operation is now being transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the LUN.

After outputting the desired number of bytes from the cache register, it is possible to either begin an additional READ PAGE CACHE-series (31h, 00h-31h) operation or to issue the READ PAGE CACHE LAST (3Fh) command.

If an additional READ PAGE CACHE-series (31h, 00h-31h) command is issued, R/B# goes LOW on the target and RDY = "0" and ARDY = "0" on the LUN for tRCBSY while the data register is copied to the cache register, then the next page begins copying into the data register. After tRCBSY, R/B# goes HIGH and RDY = "1" and ARDY = "0", indicating that the cache register is available for data output and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the cache register.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target and RDY = "0" and ARDY = "0" on the LUN for tRCBSY while the data register is copied into the cache register. After tRCBSY, R/B# goes HIGH and RDY = "1" and ARDY = "1", indicating that the cache register is available and that the LUN is ready. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the LUN busy time, tRCBSY, when RDY = "0" and ARDY = "0," the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = "1" and ARDY = "0," the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh).

READ MODE 00h

The READ MODE (00h) command disables status output and enables data output for the last selected LUN and cache register after a READ operation (00h-30h, 00h-3Ah, 00h-35h) has been monitored with a STATUS operation (70h, 78h). This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = "1" and ARDY = "0").

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN prior to the issue of the READ MODE (00h) command. This prevents bus contention.

READ PAGE 00h-30h

The READ PAGE (00h-30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1").

To read a page from the NAND Flash array, write the 00h command to the command register, the write 5 address cycles to the address registers, and conclude with the 30h command. The selected LUN will go busy (RDY = "0", ARDY = "0") for tR as data is transferred.

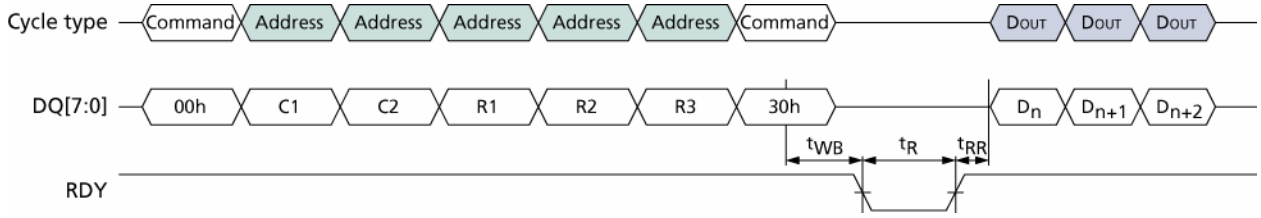
To determine the progress of the data transfer, the host my monitor the target's R/B# signal, or alternatively the status operations (70h, 78h) may be used. If the status operations are used to monitor the LUN's status, when the LUN is ready (RDY = "1", ARDY = "1") the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE WRITE COLUMN (85h).

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the LUN is ready (RDY = "1", ARDY = "1"), data output is enabled for the cache register linked to the plane addressed in the READ PAGE (00h-30h) command. When the host requests data output, it begins at the column address last specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the SELECT CACHE REGISTER (06h-E0h) command. Additionally, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 40: READ PAGE (00h-30h) Operation



READ PAGE CACHE SEQUENTIAL 31h

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = "1" and ARDY = "0").

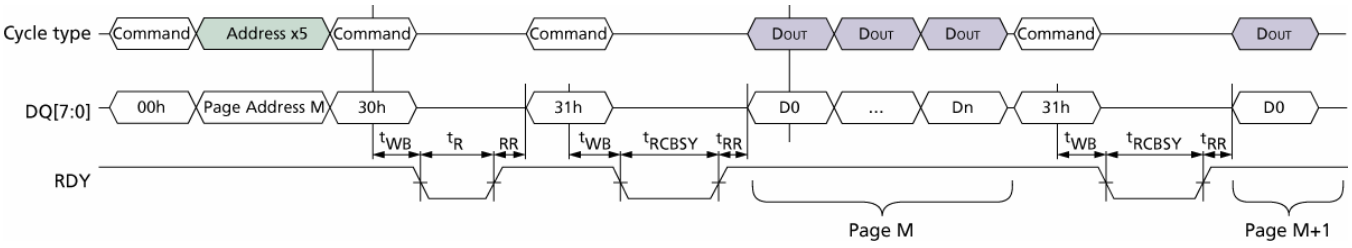
To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the LUN is busy (RDY = 0", ARDY = "0") for tRCBSY. After tRCBSY, R/B# goes HIGH and the LUN is busy with a cache operation (RDY = "1", ARDY = "0"), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

Do not issue the READ PAGE CACHE SEQUENTIAL (31h) command after reading the last page of the block into the data register. Instead, issue the READ PAGE CACHE LAST (3Fh) command. Crossing block boundaries with the READ PAGE CACHE SEQUENTIAL (31h) command is prohibited.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command followed by the READ MODE (00h) command must be used to select only one LUN and prevent bus contention.

Use of the SELECT CACHE REGISTER (06h-E0h) command is prohibited following the READ PAGE CACHE SEQUENTIAL (31h) command.

Figure 41: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM 00h-31h

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = "1" and ARDY = "0").

To issue this command, write 00h to the command register, then write 5 address cycles to the address register, and conclude by writing 31h to the command register.

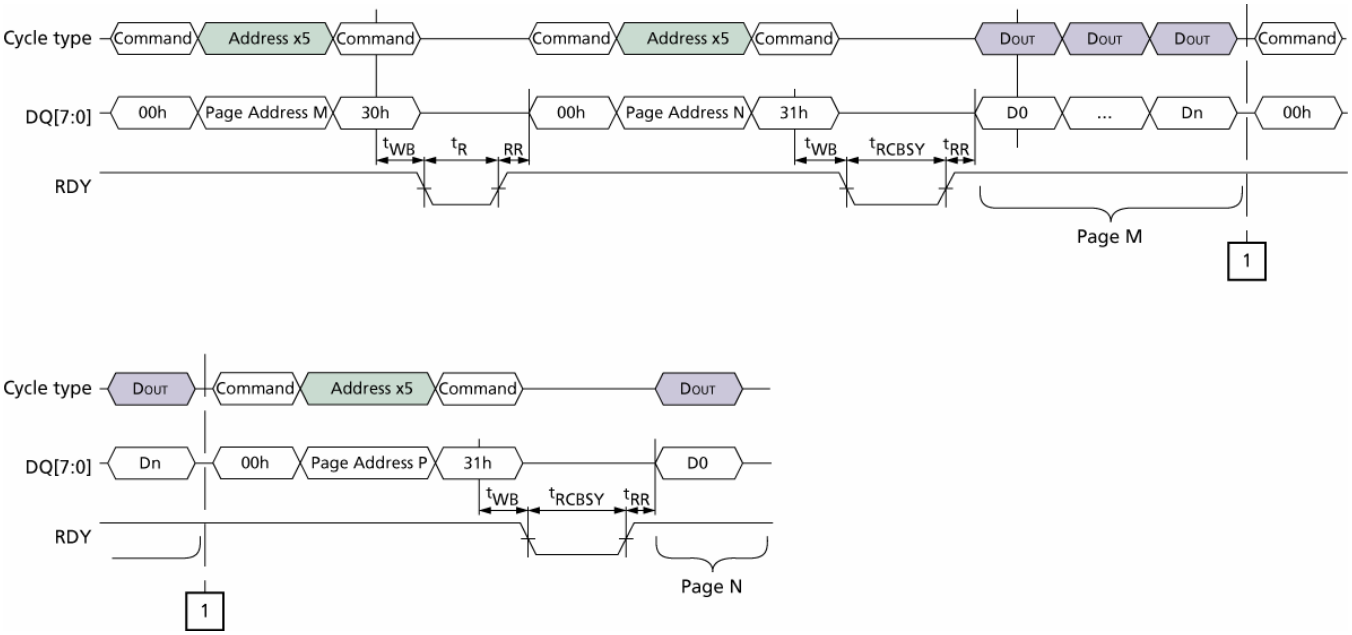
The column address in the address specified is ignored. The LUN address must match the same LUN address as the previous READ PAGE (00h-31h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

After this command is issued, R/B# goes LOW and the LUN is busy (RDY = 0", ARDY = "0") for tRCBSY. After tRCBSY, R/B# goes HIGH and the LUN is busy with a cache operation (RDY = "1", ARDY = "0"), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command followed by the READ MODE (00h) command must be used to select only one LUN and prevent bus contention.

Use of the SELECT CACHE REGISTER (06h-E0h) command is prohibited following the READ PAGE CACHE SEQUENTIAL (31h) command.

Figure 42: READ PAGE CACHE RANDOM (00h-31h) Operation



READ PAGE CACHE LAST 3Fh

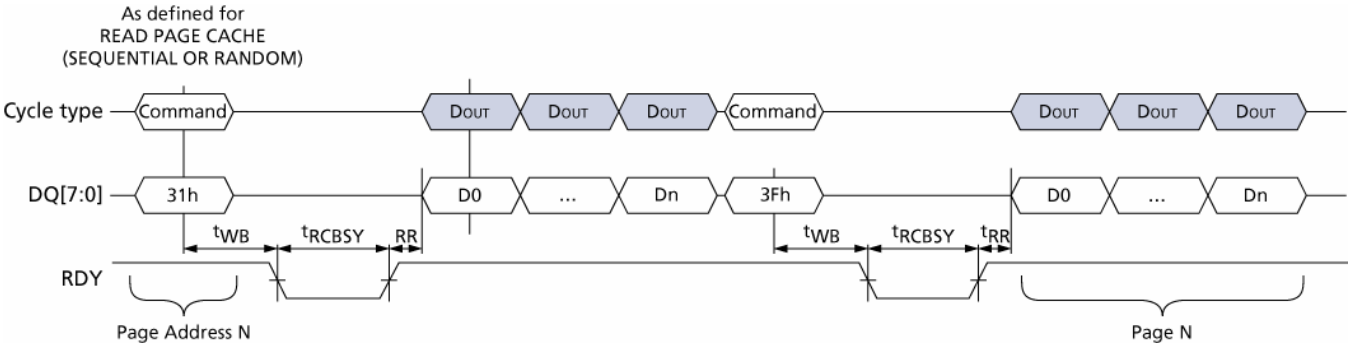
The READ PAGE CACHE LAST (3Fh) command ends the READ PAGE CACHE sequence and copies a page from the data register to the cache register. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = "1" and ARDY = "0").

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the LUN is busy (RDY = "0", ARDY = "0") for tRCBSY. After tRCBSY, R/B# goes HIGH and the LUN is ready (RDY = "1", ARDY = "1"). At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command

can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command followed by the READ MODE (00h) command must be used to select only one LUN and prevent bus contention.

Figure 43: READ PAGE CACHE LAST (3Fh) Operation



READ PAGE MULTI-PLANE 00h-32h

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND array to its cache register. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To select the final plane and to begin the read operation for all previously queued planes, issue the READ PAGE (00h-30h) command. All queued planes will transfer data from the NAND array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write 5 address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

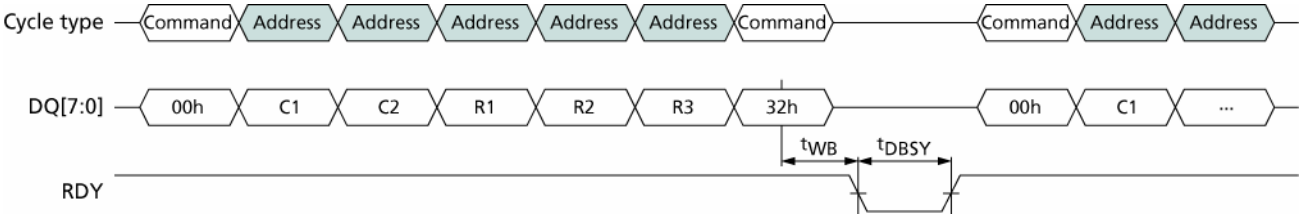
After this command is issued, R/B# goes LOW and the LUN is busy (RDY = "0", ARDY = "0") for tDBSY. After tDBSY, R/B# goes HIGH and the LUN is ready (RDY = "1", ARDY = "1"). At this point, the LUN and block are queued for data transfer from the array to the cache register for the addressed plane. During tDBSY the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following tDBSY to continue the multi-plane read operation the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), and READ PAGE (00h-30h).

If desired, additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue an additional planes for data transfer.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the LUN is ready (RDY = "1", ARDY = "1"), data output is enabled for the cache register linked to the plane addressed in the READ PAGE (00h-30h) command. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the SELECT CACHE REGISTER (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

For the READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) commands, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 44: READ PAGE MULTI-PLANE (00h-32h) Operation



Program Operations

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, …, 127). Programming pages out of order within a block is prohibited.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND array. Once the LUN is ready (RDY = "1", ARDY = "1"), the host should check the FAIL bit to very that this operation completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve system performance of program operations. When this command issued the LUN goes busy (RDY = "0", ARDY = "0") while the cache register contents are copied to the data register. Then the LUN is busy with a program cache operation (RDY = "1", ARDY = "0"). While the contents of the data register are moved to the NAND array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

To begin a Program Page Cache sequence, begin by issuing the PROGRAM PAGE CACHE (80h-15h) command. R/B# goes LOW during tCBSY and the selected LUN is busy (RDY = "0", ARDY = "0"). After tCBSY, R/B# is HIGH and RDY = "1", ARDY = "0," indicating that a program cache operation is ongoing. At this point, the following commands can be used:

- PROGRAM PAGE CACHE (80h-15h) to queue another page for a program cache operation, or
- PROGRAM PAGE (80h-10h) to queue the final page of a program cache operation.

After the second and subsequent PROGRAM PAGE CACHE (80h-15h) commands have been issued and after tCBSY the host should issue a status (70h, 78h) command to verify that the previous PROGRAM PAGE CACHE (80h-15h) command completed successfully. When RDY = "1" the FAILC bit is valid, which represents the status of the prior operation.

Ideally the final command of a Program Page Cache sequence is the PROGRAM PAGE (80h-10h). R/B# goes LOW and RDY = "0" and ARDY = "0" on the LUN for tLPROG. Once finished, R/B# goes HIGH and RDY = "1" and ARDY = "1," indicating that all program operations are complete. The host should check the FAIL and FAILC bits to verify that the final two program operations completed successfully.

If the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a Program Page Cache sequence, the host must monitor the LUN's status register until ARDY = "1." Then the host should check the FAIL and FAILC bits to verify that the final two program operations completed successfully.

For PROGRAM PAGE CACHE-series (80h-15h) operations, during the LUN busy times, tCBSY and tLPROG, when RDY = "0" and ARDY = "0," the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = "1" and ARDY = "0," the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and RESET (FFh, FCh).

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to further system performance of program operations by allowing more than one page to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See "Multi-Plane Operations" on page 71 for more details.

Multi-Plane Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to further system performance of cache program operations by allowing more than one page to be moved from the cache registers to the data registers and while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See "Multi-Plane Operations" on page 71 for more details.

PROGRAM PAGE 80h-10h

The PROGRAM PAGE (80h-10h) command allows the host to input data to a cache register and moves the data from the cache register to the specified block and page address in the array of the selected LUN. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the LUN when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = "1", ARDY = "0").

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE READ COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = "0", ARDY = "0") for tPROG as data is transferred.

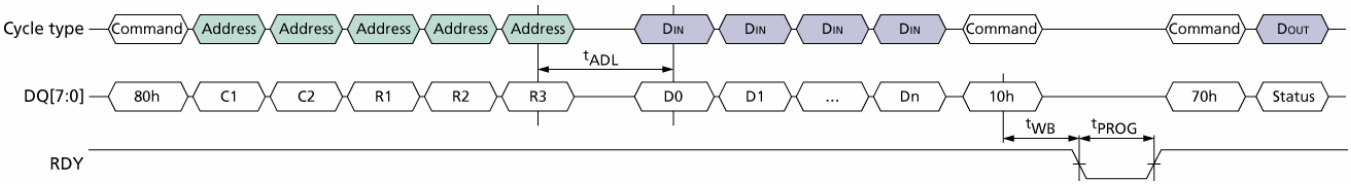
To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the status operations (70h, 78h) may be used. When the LUN is ready (RDY = "1", ARDY = "1") the host should check the status of the FAIL bit.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select

only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

The PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h). Additionally, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 45: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE CACHE 80h-15h

The PROGRAM PAGE CACHE (80h-15h) command allows the host to input data to a cache register, copies the data from the cache register to the data register, and then moves the data register contents to the specified block and page address in the array of the selected LUN. After the data is copied to the data register the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1"). It is also accepted by the LUN when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = "1", ARDY = "0").

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE READ COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = "0", ARDY = "0") for tCBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of tCBSY, the host can monitor the target's R/B# signal, or alternatively the status operations (70h, 78h) may be used. Once the LUN's status shows that it is busy with a program cache operation (RDY = "1", ARDY = "0") the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If after tCBSY the host desires to wait for the program cache operation to complete without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is "1." At this point, the host should check the status of the FAIL and FAILC bits.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the corresponding data registers and then moved to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h). Additionally, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 46: PROGRAM PAGE CACHE (80h-15h) Operation (Start)

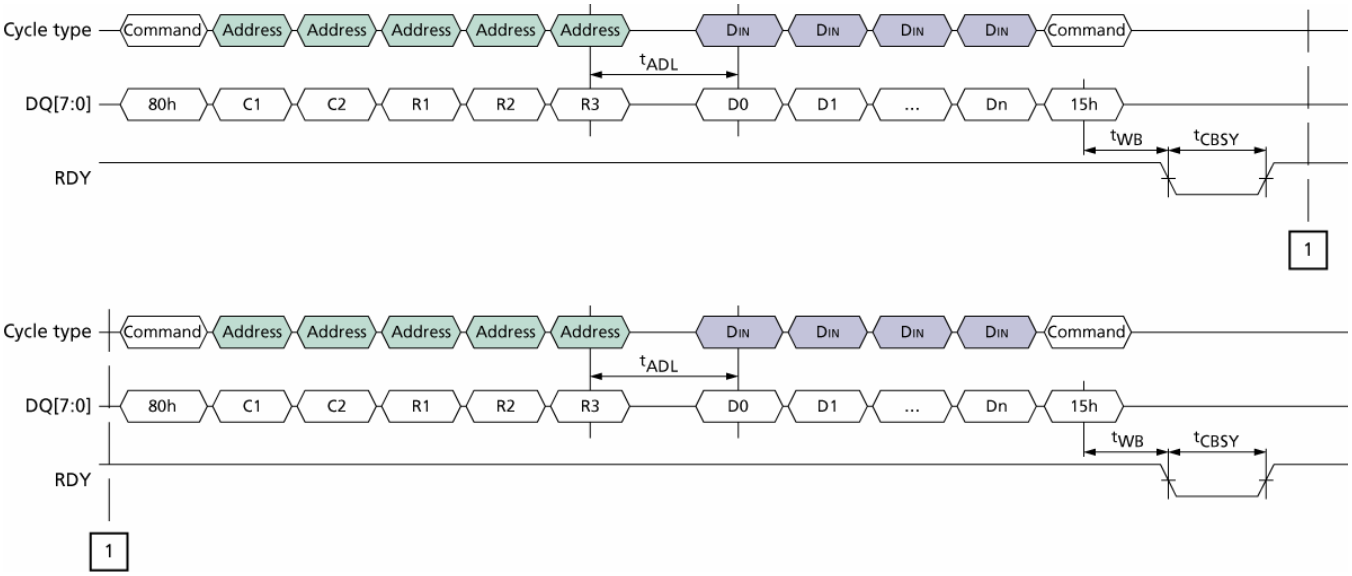
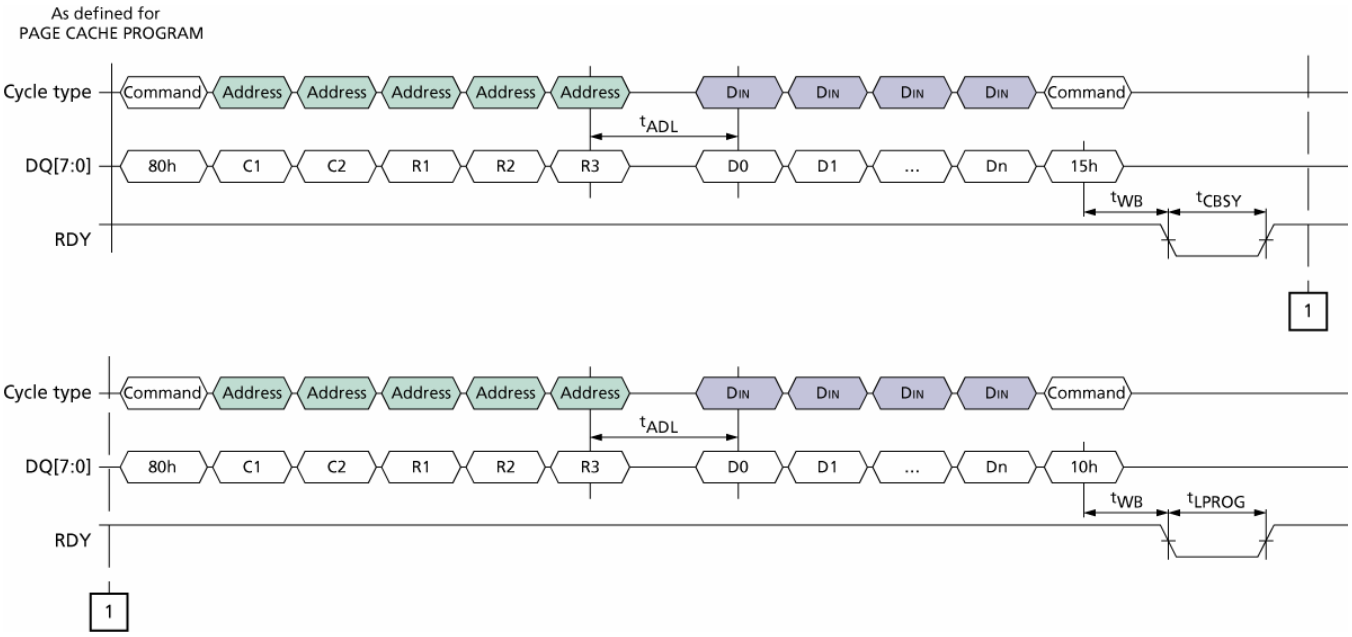


Figure 47: PROGRAM PAGE CACHE (80h-15h) Operation (End)



PROGRAM PAGE MULTI-PLANE 80h-11h

The PROGRAM PAGE MULTI-PLANE (80h-11h) command allows the host to input data to the addressed plane's cache register and queue the cache register to

ultimately be moved to the NAND array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND array. This command is accepted by the LUN when it is ready (RDY = "1").

To input a page to the cache register to queue it to be moved to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE READ COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 11h to the command register. The selected LUN will go busy (RDY = "0", ARDY = "0") for tDBSY.

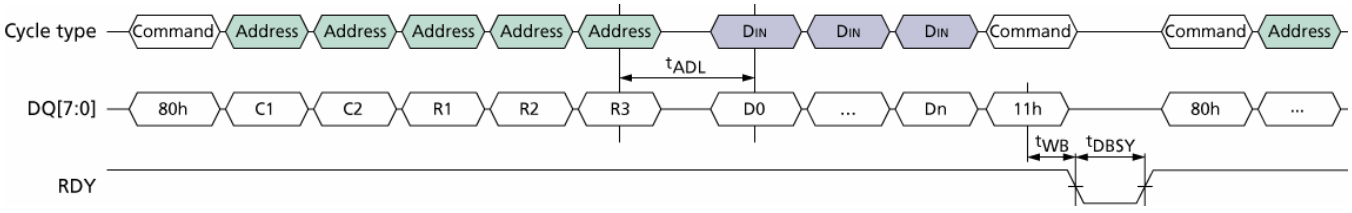
To determine the progress of tDBSY, the host can monitor the target's R/B# signal, or alternatively the status operations (70h, 78h) may be used. Once the LUN's status shows that it is ready (RDY = "1"), additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the cache registers to the NAND array for all of the addressed planes during tPROG. When the LUN is ready (RDY = "1", ARDY = "1"), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation, data is transferred once previous array operations finish, from the cache registers to the data registers. Then it is moved from the data registers to the NAND array for all of the addressed planes. This occurs during tCBSY. After tCBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 48: PROGRAM PAGE MULTI-PLANE (80h-11h) Operation



Erase Operations

Erase operations are used to clear the contents of a block in the NAND array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND array. Once the LUN is ready (RDY = "1", ARDY = "1"), the host should check the FAIL bit to verify that this operation completed successfully.

Multi-Plane Erase Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See "Multi-Plane Operations" on page 71 for more details.

ERASE BLOCK 60h-D0h

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND array. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1").

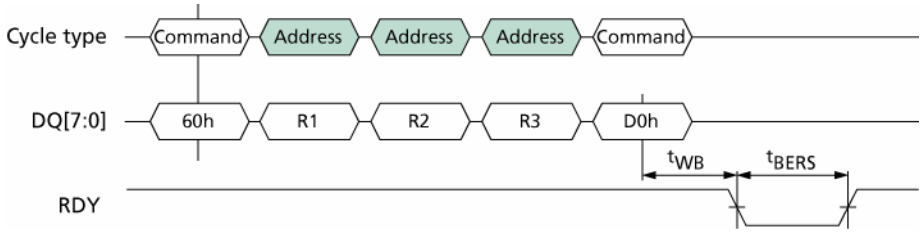
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected LUN will go busy (RDY = "0", ARDY = "0") for tBERS the block is erased.

To determine the progress of operation, the host can monitor the target's R/B# signal, or alternatively the status operations (70h, 78h) may be used. When the LUN is ready (RDY = "1", ARDY = "1") the host should check the status of the FAIL bit.

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a multi-plane erase operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). Additionally, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 49: ERASE BLOCK (60h-D0h) Operation



ERASE BLOCK MULTI-PLANE 60h-D1h

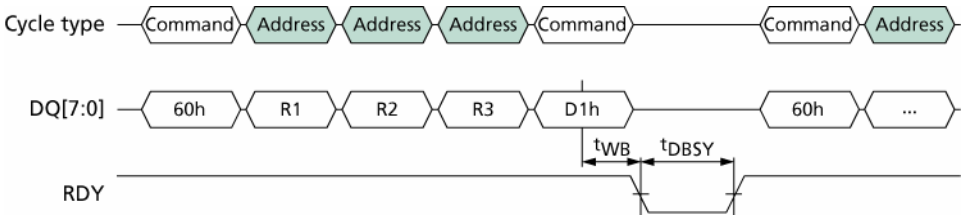
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the erase operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the LUN when it is ready (RDY = "1", ARDY = "1").

To queue a block to be erased, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected LUN will go busy (RDY = "0", ARDY = "0") for tDBSY.

To determine the progress of tDBSY, the host can monitor the target's R/B# signal, or alternatively the status operations (70h, 78h) may be used. Once the LUN's status shows that it is ready (RDY = "1", ARDY = "1"), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see "Multi-Plane Addressing" on page 72 for multi-plane addressing requirements.

Figure 50: ERASE BLOCK MULTI-PLANE (60h-D1h) Operation



Copyback Operations

Copyback operations provide the ability to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear-leveling.

The Copyback operation is a two-step process consisting of COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands. To move one page from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. Once the LUN is ready (RDY = "1", ARDY = "1"), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. Once the LUN is ready (RDY = "1", ARDY = "1"), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple Copyback operations it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. Then when the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE WRITE COLUMN (85h) command can be used to change the column address.

It is not possible to use the Copyback Operation to move data from one plane to another or from one LUN to another. Instead this is accomplished using a READ PAGE (00h-30h) command, reading the data out of the part, and then using a PROGRAM PAGE (80h-10h) command to program the data to a new plane or LUN.

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands the following commands are permitted: Status Operations (70h, 78h), and Column Address Operations (05h-E0h, 06h-E0h, 85h). Reset Operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices that have more than one LUN per target, once COPYBACK READ (00h-35h) is issued, Multi-LUN operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

Multi-Plane Copyback Operations

Multi-Plane Copyback Read operations improve read data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of Copyback Program operations by allowing more than one page to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command.

See "Multi-Plane Operations" on page 71 for more details.

COPYBACK READ 00h-35h

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except 35h is written to the command register instead of 30h. See "READ PAGE 00h-30h" on page 55 for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 51: COPYBACK READ (00h-35h) Operation

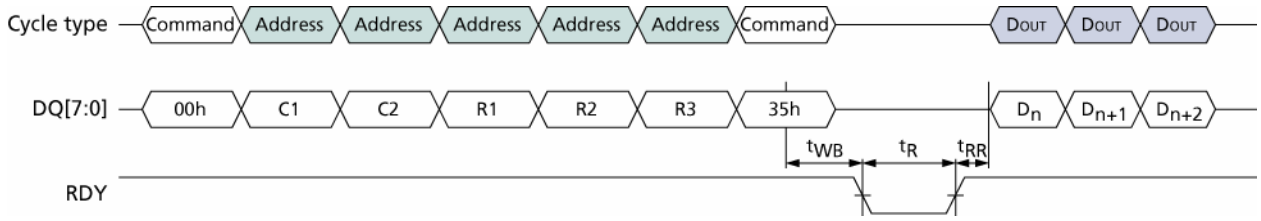
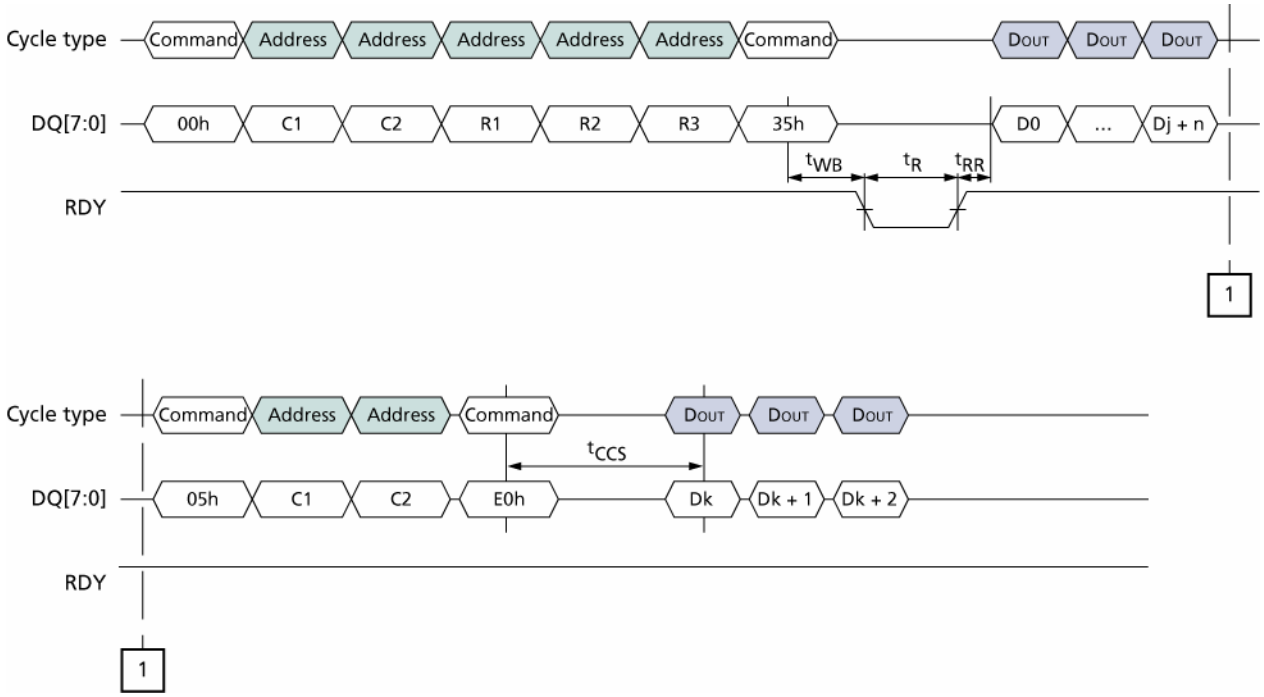


Figure 52: COPYBACK READ (00h-35h) with CHANGE READ COLUMN (05h-E0h)



COPYBACK PROGRAM 85h-10h

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See "PROGRAM PAGE 80h-10h" on page 60 for further details.

Figure 53: COPYBACK PROGRAM (85h-10h) Operation

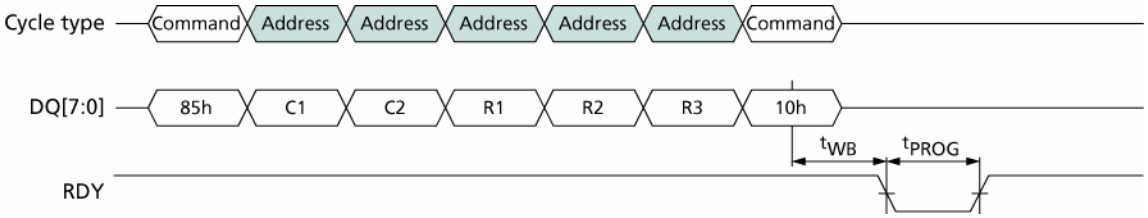
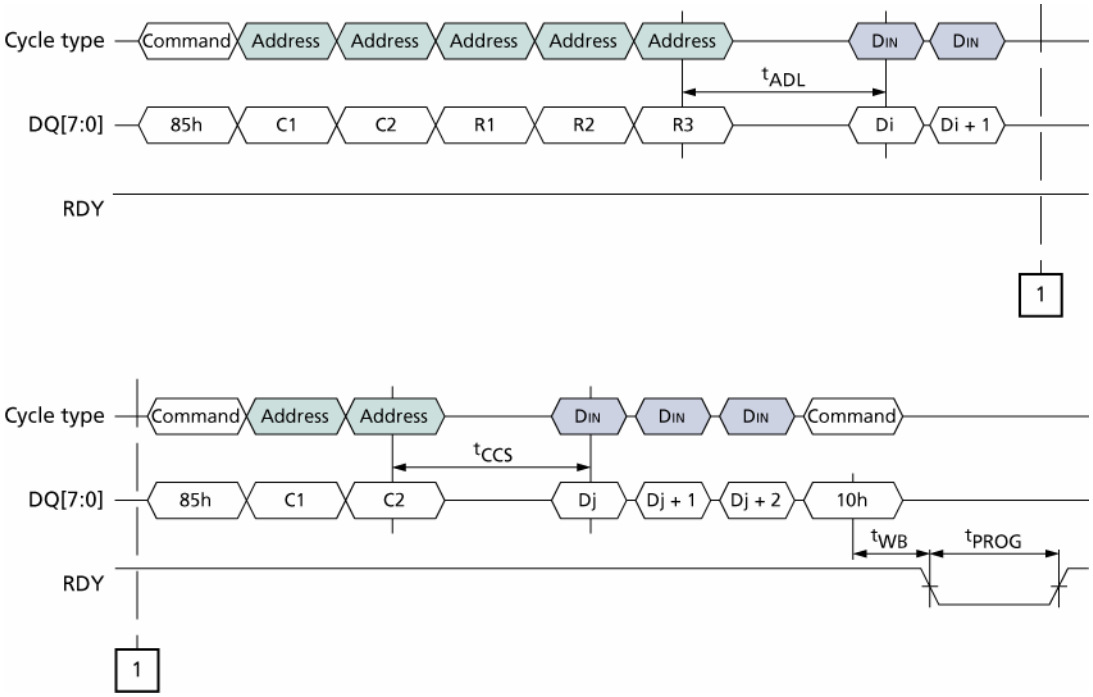


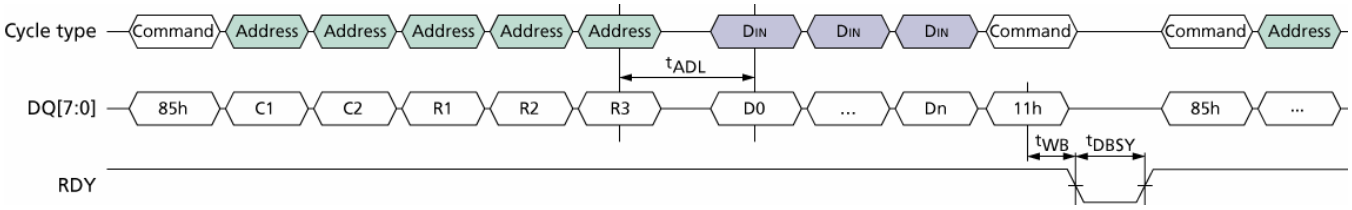
Figure 54: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation



COPYBACK PROGRAM MULTI-PLANE 85h-11h

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (85h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See "PROGRAM PAGE MULTI-PLANE 80h-11h" on page 62 for further details.

Figure 55: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (4,320 bytes per page) of OTP data are available on the target, and the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in an erased state (all bits are "1"). Programming enables the user to program only "0" bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as "one-time programmable," Micron provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by 3 cycles of 00h to P2 through P4.

When the device is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area. The OTP area is assigned to page addresses 02h through 0Bh.

OTP programming and protection are achieved in two discrete operations. Each page in the OTP area is programmed using the PROGRAM OTP PAGE (80h-10h) command. The pages in the OTP area (02h-0Bh) must be programmed in ascending order.

To protect the OTP area, issue the 80h command followed by five address cycles (00h-00h-01h-00h-00h), followed by the 10h command. R/B# goes LOW for tPROG.

To read pages in the OTP area, whether or not it is protected, issue the PAGE READ (00h-30h) command.

Erase commands are not valid while the device is in OTP operation mode.

To exit OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the host device issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the device will be busy for tOBSY and the WP# status register bit is "0," meaning that the page is write-protected.

If the host device issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid.

To determine whether or not the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the SELECT LUN WITH STATUS (78h) command is prohibited while the OTP operation mode is active.

If the RESET (FFh) command is issued while in the OTP operation mode, the device will remain in the OTP operation mode. If the device is in the synchronous interface it will change to the asynchronous interface.

If the SYNCHRONOUS RESET (FCh) command is issued while in the OTP operation mode, the device will remain in the OTP operation mode.

PROGRAM OTP PAGE 80h-10h

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. An entire page is programmed at one time. To program data in the OTP area, the device must be in OTP operation mode.

To use the PROGRAM PAGE command, issue the 80h command. Issue 5 ADDRESS cycles: the first 2 ADDRESS cycles are the column address, and for the remaining 3 cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, tPROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the SELECT LUN WITH STATUS (78h) command is prohibited.

When the device is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Table 14 on page 49).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGE WRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, R/B# goes LOW for tOBSY. After tOBSY the status register is set to 60h.

It is possible to program each OTP page a maximum of one time.

Figure 56: PROGRAM OTP PAGE (80h-10h)Operation

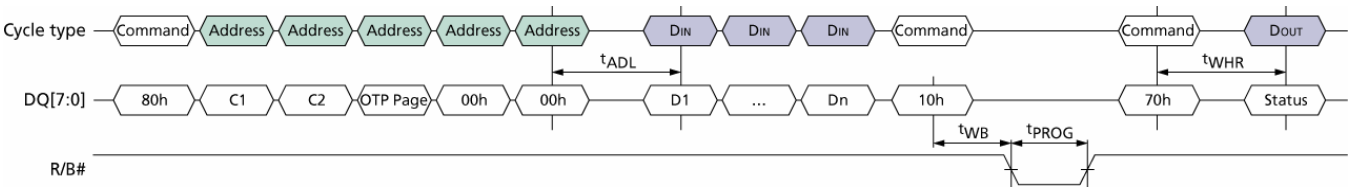
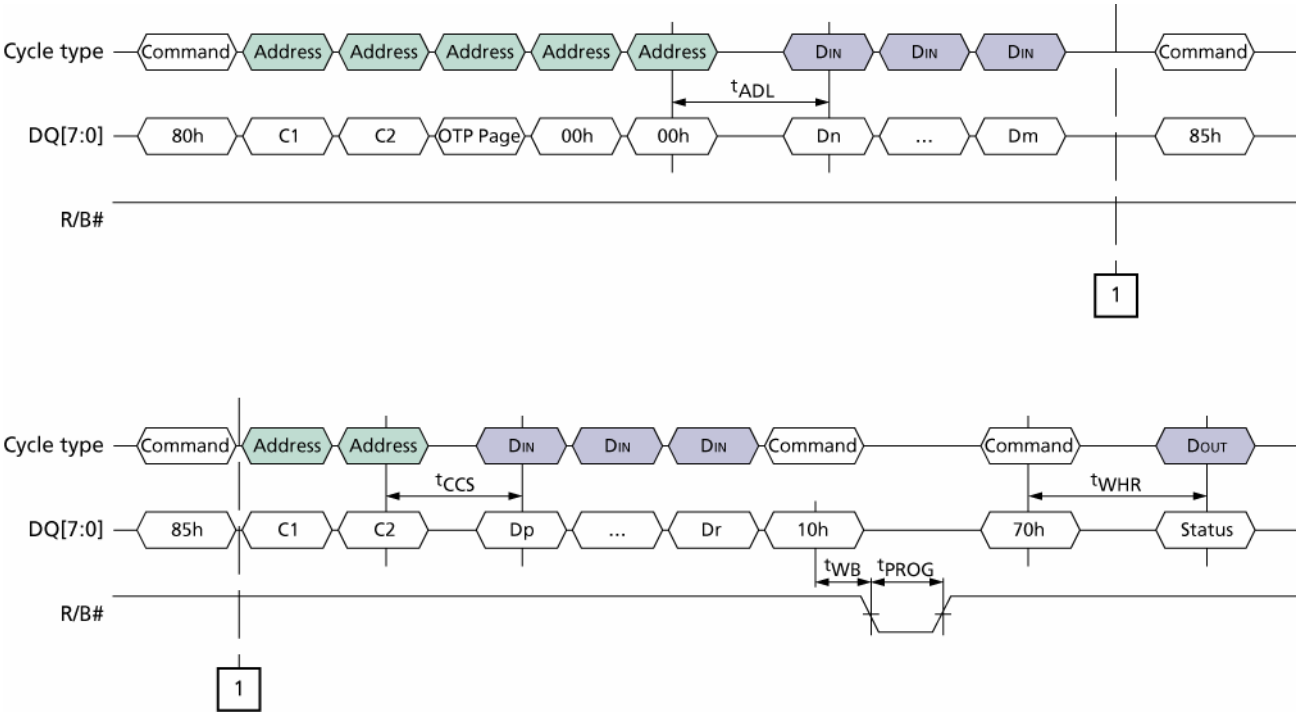


Figure 57: PROGRAM OTP PAGE (80h-10h) Operation with CHANGE WRITE COLUMN (85h)



PROTECT OTP AREA 80h-10h

To protect all data in the OTP area, set the device to OTP operation mode, then issue the PROTECT OTP AREA (80h-10h) command to page 1 in block 0. Data input cycles are not required.

After the OTP AREA is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

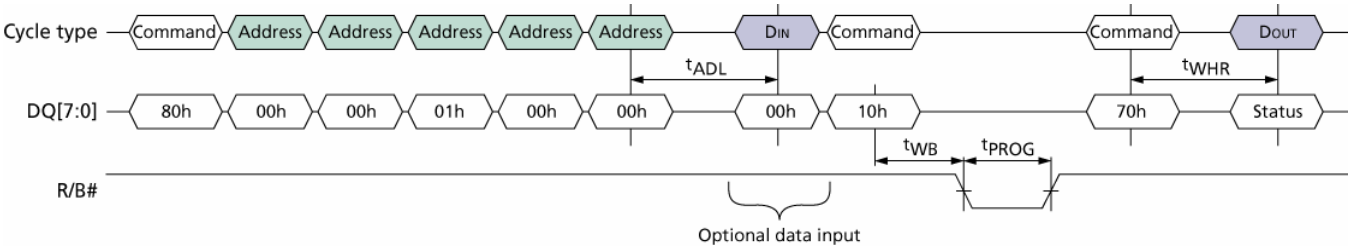
To use the PROTECT OTP AREA (80h-10h) command to protect the OTP area, issue the 80h command. Next, issue the following 5 address cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, tPROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the SELECT LUN WITH STATUS (78h) command is prohibited.

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for tOBSY. After tOBSY the status register is set to 60h.

When the device is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Table 14 on page 49).

Figure 58: PROTECT OTP AREA (80h-10h) Operation



1. OTP data is protected following a "pass" status confirmation.

READ OTP PAGE 00h-30h

To read data from the OTP area, set the device to OTP operation mode, then issue the READ OTP PAGE (00h-30h) command. Data can be read from OTP pages within the OTP area whether or not the area is protected.

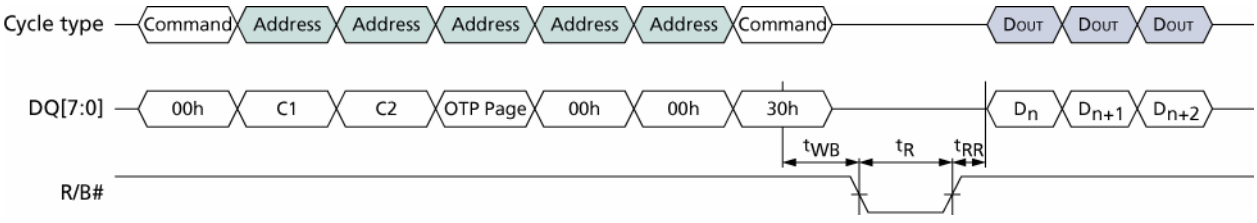
To use the READ OTP PAGE (00h-30h) command for reading data from the OTP area, issue the 00h command. Next, issue five address cycles: the first 2 address cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Finally, issue the 30h command. The selected LUN will go busy (RDY = "0", ARDY = "0") for tR as data is transferred.

To determine the progress of the data transfer, the host my monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command may be used. If the status operations are used to monitor the LUN's status, when the LUN is ready (RDY = "1", ARDY = "1") the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

Additional pages within the OTP area can be selected by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the SELECT LUN WITH STATUS (78h) and SELECT CACHR REGISTER (06h-E0h) commands are prohibited.

Figure 59: READ OTP PAGE (00h-30h) Operation



Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes.

The planes are addressed via the low-order block address bits. Specific details are provided in Figure 8 and Table 2 on page 13.

Multi-plane operations make better use of the Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on more than one plane, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a program operation on one plane with an erase operation on another.

When issuing multi-plane program page or multi-plane erase block operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates an error occurred (FAIL = "1" and/or FAILC = "1"), use the SELECT LUN WITH STATUS (78h) command—once for each plane— to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require multiple 5-cycle addresses, one address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit(s), BA[8:7], must be different for each issued address.
- The page address bits, PA[6:0], must be identical for all of the issued addresses.

The READ STATUS (70h) command should be used following multi-plane program page and erase block operations on a single LUN.

Multi-LUN Operations

In devices that have more than one LUN per target, it is possible to improve performance by interleaving operations between the LUNs. A Multi-LUN operation is one that is issued to an idle LUN (RDY = "1") while another LUN is busy (RDY = "0").

Multi-LUN operations are prohibited following Reset (FFh, FCh), Identification (90h, ECh, EDh), and Configuration (EEh, EFh) operations until ARDY = "1" for all of the LUNs on the target.

During a Multi-LUN operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the LUNs have finished their operations. R/B# remains LOW while any LUN is busy. When R/B# goes HIGH, then all of the LUNs are idle and the operations are complete. Alternatively, the SELECT LUN WITH STATUS (78h) command can report the status of each LUN individually.

If a LUN is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h) or TWO-PLANE PROGRAM PAGE CACHE (80h-11h-80h-15h), then the LUN is able to accept the data for another cache operation when status register bit 6 is "1." All operations, including cache operations, are complete on a die when status register bit 5 is "1."

During and following Multi-LUN operations, the READ STATUS (70h) command is prohibited. Instead, use the SELECT LUN WITH STATUS (78h) command to monitor status. This command selects which LUN will report status. When Multi-Plane commands are used with Multi-LUN operations, the multi-plane commands must also meet the requirements in "Multi-Plane Operations" on page 71.

See Table 5 on page 34 for the list of which commands can be issued while other LUNs are busy.

During a Multi-LUN operation that involves a Program-series (80h-10h, 80h-15h, 80h-11h) operation and a Read operation, the Program-series operation must be

issued before the Read-series operation. The data from the Read-series operation must be output to the host before the next Program-series operation is issued. This is because the 80h command clears the cache register contents of all of the cache registers on all of the planes.

Error Management

Each NAND Flash LUN is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the LUNs may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks may develop with use. However, the total number of available blocks per LUN will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See Table 15 for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after a PROGRAM or ERASE operation.
- Under typical conditions, use the minimum required ECC shown in Table 15.
- Use bad-block management and wear-leveling algorithms.

Table 15: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	1,998
Total available blocks per LUN	2,048
First spare area location	Byte 4,096
Bad-block mark	00h
Minimum required ECC	8-bit ECC per 540 bytes of data

Output Drive Strength

Because High Speed NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four allowable settings for the output drivers – Overdrive 2, Overdrive 1, Nominal, and Underdrive.

The Nominal output drive strength setting is the power-on default value. The host is able to select a different drive strength setting using the SET FEATURES (EFh) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 16: Output Drive Strength Test Conditions

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	–25°C
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	+85°C

Table 17: Output Drive Strength Impedance Values

Output Strength	Rpd/Rpu	VOUT to VssQ	Minimum	Nominal	Maximum	Units
Overdrive 2	Rpd	VccQ × 0.2	7.5	13.5	34.0	ohms
		VccQ × 0.5	9.0	18.0	31.0	ohms
		VccQ × 0.8	11.0	23.5	44.0	ohms
	Rpu	VccQ × 0.2	11.0	23.5	44.0	ohms
		VccQ × 0.5	9.0	18.0	31.0	ohms
		VccQ × 0.8	7.5	13.5	34.0	ohms
Overdrive 1	Rpd	VccQ × 0.2	10.5	19.0	47.0	ohms
		VccQ × 0.5	13.0	25.0	44.0	ohms
		VccQ × 0.8	16.0	32.5	61.5	ohms
	Rpu	VccQ × 0.2	16.0	32..5	61.5	ohms
		VccQ × 0.5	13.0	25.0	44.0	ohms
		VccQ × 0.8	10.5	19.0	47.0	ohms
Nominal	Rpd	VccQ × 0.2	15.0	27.0	66.5	ohms
		VccQ × 0.5	18.0	35.0	62.5	ohms
		VccQ × 0.8	22.0	52.0	88.0	ohms
	Rpu	VccQ × 0.2	22.0	52.0	88.0	ohms
		VccQ × 0.5	18.0	35.0	62.5	ohms
		VccQ × 0.8	15.0	27.0	66.5	ohms
Underdrive	Rpd	VccQ × 0.2	21.5	39.0	95.0	ohms
		VccQ × 0.5	26.0	50.0	90.0	ohms
		VccQ × 0.8	31.5	66.5	126.5	ohms
	Rpu	VccQ × 0.2	31.5	66.5	126.5	ohms
		VccQ × 0.5	26.0	50.0	90.0	ohms
		VccQ × 0.8	21.5	39.0	95.0	ohms

Table 18: Pull-up and Pull-down Output Impedance Mismatch

Drive Strength	Min	Max	Unit	Notes
Overdrive 2	0	6.3	ohms	1, 2
Overdrive 1	0	8.8	ohms	1, 2
Nominal	0	12.3	ohms	1, 2
Underdrive	0	17.5	ohms	1, 2

1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: VccQ = VccQ(min), Vout = VccQ × 0.5, TA = TOPER

AC Overshoot/Undershoot Specifications

The permitted AC overshoot and undershoot area depends on the timing mode selected by the host.

Table 19: Overshoot / Undershoot Parameters

Parameter	Timing Mode					Unit
	0 (50ns)	1 (30ns)	2 (20ns)	3 (15ns)	4 (12ns)	
Maximum peak amplitude allowed for overshoot area	1.0	1.0	1.0	1.0	1.0	V
Maximum peak amplitude allowed for undershoot area	1.0	1.0	1.0	1.0	1.0	V
Maximum overshoot area above VccQ	3.0	3.0	3.0	2.25	1.80	V-ns
Maximum undershoot area below VssQ	3.0	3.0	3.0	2.25	1.80	V-ns

Figure 60: Overshoot

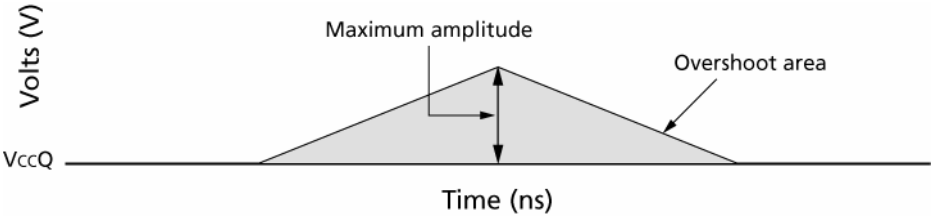
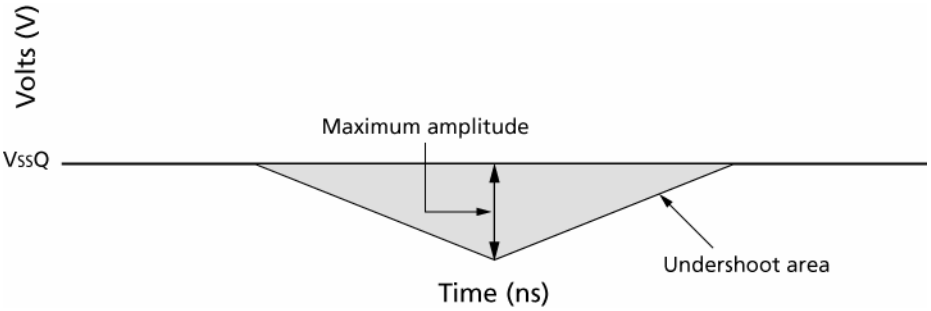


Figure 61: Undershoot



Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1V/ns it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100 percent tested. If using slew rates slower than the minimum values, timing must be derated by the host.

Table 20: Test Conditions for Input Slew Rate

Parameter	Value
Rising Edge	V_{IL} (DC) to V_{IH} (AC)
Falling Edge	V_{IH} (DC) to V_{IL} (AC)
Temperature Range	T_A

Table 21: Input Slew Rate

Description	Timing Mode					Unit	Notes
	0 (50ns)	1 (30ns)	2 (20ns)	3 (15ns)	4 (12ns)		
Input slew rate (MIN)	0.5	0.5	0.5	0.5	0.5	V/ns	
Derating factor for setup times	TBD	TBD	TBD	TBD	TBD	ps per 100mV	
Derating factor for hold times	TBD	TBD	TBD	TBD	TBD	ps per 100mV	

Output Slew Rate

The output slew rate is tested using the following setup with only one die per I/O channel.

Table 22: Test Conditions for Output Slew Rate

Parameter	Value
Rising Edge	V_{IL} (DC) to V_{IH} (AC)
Falling Edge	V_{IH} (AC) to V_{IL} (DC)
Output Capacitive Load (C_{LOAD})	5pF
Temperature Range	T_A

Table 23: Output Slew Rate

Output Drive Strength	Min	Max	Unit
Overdrive 2	1.0	5.5	V/ns
Overdrive 1	0.85	5.0	V/ns
Nominal	0.75	4.0	V/ns
Underdrive	0.60	4.0	V/ns

Electrical Characteristics

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 24: Absolute Maximum Ratings by Device

Voltage on any pin relative to V_{SS}.

Parameter	Symbol	Min	Max	Unit
Voltage input	V_{IN}	–0.6	+4.6	V
VCC supply voltage	V_{CC}	–0.6	+4.6	V
VCCQ supply voltage	V_{CCQ}	–0.6	+4.6	V
Storage temperature	T_{STG}	–65	+150	°C

Table 25: Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	—	+70	°C
	Wireless		–25	—	+85	
V_{CC} supply voltage		V_{CC}	2.7	3.3	3.6	V
V_{CCQ} supply voltage		V_{CCQ}	1.7	1.8	1.95	V
V_{SS} ground voltage		V_{SS}	0	0	0	V
V_{SSQ} ground voltage		V_{SSQ}	0	0	0	V

Table 26: Device DC and Operating Characteristics

All values are per LUN unless otherwise specified.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Array and I/O read current	CE# = V_{IL}; tCK = tCK (min) or tRC = tRC (min); Iout = 0mA	I_{CC1}	—	25	50	mA
Array program current	—	I_{CC2}	—	25	50	mA
Erase current	—	I_{CC3}	—	25	50	mA
I/O read current	CE# = V_{IL}; tCK = tCK (min) or tRC = tRC (min); Iout = 0mA	I_{CCQ1}	—	25	50	mA
Standby current – Vcc	CE# = VccQ – 0.2V; WP# = 0V/VccQ	I_{SB}	—	10	50	µA
Standby current – VccQ	CE# = VccQ – 0.2V; WP# = 0V/VccQ	I_{SBQ}	—	3	10	µA

Table 27: Pin Capacitance – BGA-100 Package

Description	Symbol	MT29H8G08 / MT29H16G08			MT29H32G08			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Input capacitance (CLK)	C_{CK}	3.35	3.6	3.85	5.7	6.2	6.7	pF	1, 2, 3
Input capacitance (ALE, CLE, W/R#)	C_{IN}	3.5	4.0	4.5	5.8	6.8	7.8	pF	1, 2, 3
Input/output capacitance (DQ[7:0], DQS)	C_{IO}	4.0	4.5	5.0	7.0	8.0	9.0	pF	1, 2, 3
Input capacitance (CE#, WP#)	C_{OTHER}	—	—	5		—	10	pF	1, 2
Delta clock capacitance	DC_{CK}	—	—	0.25		—	0.5	pF	1, 2
Delta input capacitance	DC_{IN}	—	—	0.50		—	1.0	pF	1, 2
Delta input/output capacitance	DC_{IO}	—	—	0.50		—	1.0	pF	1, 2

1. Verified in device characterization; not 100 percent tested.
2. Test conditions: T_A = 25°C, *f* = 100MHz, V_{IN} = 0V.
3. Values for C_{CK}, C_{IN} and C_{IO} (typ) are estimates.

Table 28: Test Conditions

Parameter	Value	Notes
Input pulse levels	0.0V to VccQ	
Input rise and fall slew rates	1V/ns	
Input and output timing levels	VccQ/2	
Output load – Synchronous interface, nominal output drive strength	C_L = 5pF	1, 2
Output load – Asynchronous interface, nominal output drive strength	1 TTL gate and C_L = 30pF	2

1. Transmission line delay is assumed to be very small.
2. This test setup applies to all package configurations (SDP, DDP, QDP).

Table 29: Device Operating Characteristics

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (R/E#), WP#	V_{IH} (AC)	0.8 × VccQ	—	VccQ + 0.3	V	
AC input low voltage		V_{IL} (AC)	–0.3	—	0.2 × VccQ	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (R/E#)	V_{IH} (DC)	0.7 × VccQ	—	VccQ + 0.3	V	1
DC input low voltage		V_{IL} (DC)	–0.3	—	0.3 × VccQ	V	1
Output high voltage	I_{OH} = –100µA	V_{OH}	VccQ – 0.1V	—	—	V	2
Output low voltage	I_{OL} = 100µA	V_{OL}	—	—	0.1	V	2
Input leakage current	Any input V_{IN} = 0V to VccQ (all other pins under test=0V)	I_{LI}	—	—	±10	µA	3
Output leakage current	I/Os are disabled; V_{OUT} = 0V to VccQ	I_{LO}	—	—	±10	µA	3
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	—	mA	

1. The DC values only apply to the synchronous interface.
2. V_{OH} and V_{OL} only apply to the asynchronous interface.
3. All leakage currents are per LUN. Two LUNs have a maximum leakage current of ±20µA and four LUNs have a maximum leakage current of ±40µA in the asynchronous interface.

Table 30: AC Characteristics: Command, Address, and Data — Synchronous Interface

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		50		30		20		15		12		ns	
Frequency		~20		~33		~50		~67		~83		MHz	
Access window of DQ[7:0] from CLK	tAC	—	20	—	20	—	20	—	20	—	20	ns	
ALE to data loading time	tADL	100	—	100	—	70	—	70	—	70	—	ns	
Cmd, Addr, Data delay	tCAD	25	—	25	—	25	—	25	—	25	—	ns	1
ALE, CLE, W/R# hold	tCALH	10	—	5	—	4	—	3	—	2.5	—	ns	
ALE, CLE, W/R# setup	tCALS	10	—	5	—	4	—	3	—	2.5	—	ns	
DQ hold – Cmd, Addr	tCAH	10	—	5	—	4	—	3	—	2.5	—	ns	
DQ setup – Cmd, Addr	tCAS	10	—	5	—	4	—	3	—	2.5	—	ns	
Change column setup	tCCS	200	—	200	—	200	—	200	—	200	—	ns	2
CE# hold	tCH	10	—	5	—	4	—	3	—	2.5	—	ns	
CLK cycle time	tCK (avg)	50	100	30	50	20	30	15	20	12	15	ns	3
CLK cycle high	tCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK	4
CLK cycle low	tCKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK	4
Data output end to W/R# HIGH	tCKWR	tCKWR (MIN) = RoundUp[(tDQSCK(MAX) + tCK) / tCK]										tCK	
CE# setup	tCS	35	—	25	—	15	—	15	—	15	—	ns	
Data In hold	tDH	5	—	2.5	—	1.7	—	1.3	—	1.1	—	ns	
Access window of DQS from CLK	tDQSCK	—	20	—	20	—	20	—	20	—	20	ns	
DQS, DQ[7:0] Driven by NAND	tDQSD	0	20	0	20	0	20	0	20	0	20	ns	
DQS, DQ[7:0] to tri-state	tDQSHZ	—	20	—	20	—	20	—	20	—	20	ns	5
DQS input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	

		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4			
DQS-DQ skew	tDQSQ	—	5	—	2.5	—	1.7	—	1.3	—	1.0	ns	
Data input	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
Data In setup	tDS	5	—	3	—	2	—	1.5	—	1.1	—	ns	
DQS falling edge from CLK rising – hold	tDSH	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	tCK	
DQS falling to CLK rising –setup	tDSS	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	tCK	
Data Valid Window	tDVW	tDVW = tQH – tDQSQ										ns	
Half Clock Period	tHP	tHP = Min(tCKH, tCKL)										ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	tQH	tQH = tHP – tQHS										ns	
Data Hold Skew Factor	tQHS	—	6	—	3	—	2	—	1.5	—	1.2	ns	
Data output to command, address, or data input	tRHW	100	—	100	—	100	—	100	—	100	—	ns	
Ready to data output	tRR	20	—	20	—	20	—	20	—	20	—	ns	
Device reset time (Read / Program / Erase)	tRST	—	5/10/500	—	5/10/500	—	5/10/500		5/10/500	—	5/10/500	µs	6
CLK high to R/B# low	tWB	—	100	—	100	—	100	—	100	—	100	ns	
Command cycle to data output	tWHR	80	—	60	—	60	—	60	—	60	—	ns	
DQS write preamble	tWPRE	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	tCK	
DQS write postamble	tWPST	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	tCK	
W/R# LOW to data output cycle	tWRCK	20	—	20	—	20	—	20	—	20	—	ns	
WP# transition to command cycle	tWW	100	—	100	—	100	—	100	—	100	—	ns	

1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. This value is specified in the parameter page.
3. tCK(avg) is the average clock period over any consecutive 200-cycle window.
4. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
5. tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
6. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5µs.

Table 31: AC Characteristics: Command, Address, and Data — Asynchronous Interface

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Min	Max	Max	Min	Max		
Clock Period		100		50		35		30		25		ns	
Frequency		~10		~20		~28		~33		~40		MHz	
ALE to data start	tADL	200	—	100	—	100	—	100	—	70	—	ns	1
ALE hold time	tALH	20	—	10	—	10	—	5	—	5	—	ns	
ALE setup time	tALS	50	—	25	—	15	—	10	—	10	—	ns	
ALE to RE# delay	tAR	25	—	10	—	10	—	10	—	10	—	ns	
CE# access time	tCEA	—	100	—	45	—	30	—	25	—	25		
Change column setup time	tCCS	200	—	200	—	200	—	200	—	200	—	ns	
CE# hold time	tCH	20	—	10	—	10	—	5	—	5	—	ns	
CE# high to output high-Z	tCHZ	—	100	—	50	—	50	—	50	—	30	ns	2
CLE hold time	tCLH	20	—	10	—	10	—	5	—	5	—	ns	
CLE to RE# delay	tCLR	20	—	10	—	10	—	10	—	10	—	ns	
CLE setup time	tCLS	50	—	25	—	15	—	10	—	10	—	ns	
CE# high to output hold	tCOH	0	—	15	—	15	—	15	—	15	—	ns	
CE# setup time	tCS	70	—	35	—	25	—	25	—	20	—	ns	
Data hold time	tDH	20	—	10	—	5	—	5	—	5	—	ns	
Data setup time	tDS	40	—	20	—	15	—	10	—	10	—	ns	
Output high-Z to RE# low	tIR	10	—	0	—	0	—	0	—	0	—	ns	

		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4			
RE# cycle time	tRC	100	—	50	—	35	—	30	—	25	—	ns	
RE# access time	tREA	—	40	—	30	—	25	—	20	—	20	ns	3
RE# high hold time	tREH	30	—	15	—	15	—	10	—	10	—	ns	3
RE# high to output hold	tRHOH	0	—	15	—	15	—	15	—	15	—	ns	3
RE# high to WE# low	tRHW	200	—	100	—	100	—	100	—	100	—	ns	
RE# high to output high-Z	tRHZ	—	200	—	100	—	100	—	100	—	100	ns	2, 3
RE# low to output hold	tRLOH	0	—	0	—	0	—	0	—	5	—	ns	3
RE# pulse width	tRP	50	—	25	—	17	—	15	—	12	—	ns	
Ready to RE# low	tRR	40	—	20	—	20	—	20	—	20	—	ns	
Device reset time (Read / Program / Erase)	tRST	—	5/10/ 500	—	5/10/ 500	—	5/10 /500		5/10/ 500	—	5/10/ 500	µs	4, 5
WE# high to R/B# low	tWB	—	200	—	100	—	100	—	100	—	100	ns	6
WE# cycle time	tWC	100	—	45	—	35	—	30	—	25	—	ns	
WE# high hold time	tWH	30	—	15	—	15	—	10	—	10	—	ns	
WE# high to RE# low	tWHR	120	—	80	—	80	—	60	—	60	—	ns	
WE# pulse width	tWP	50	—	25	—	17	—	15	—	12	—	ns	
WP# transition to WE# low	tWW	100	—	100	—	100	—	100	—	100	—	ns	

1. Timing for tADL begins in the ADDRESS cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input.
2. Data transition is measured ±200mV from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if output drive strength is not set to at least Nominal.
4. If RESET (FFh) command is issued when the target is ready, the target goes busy for a maximum of 5µs.
5. See Table 33 on page 85 for details on the power-on reset time, tPOR.

6. Do not issue a new command during tWB, even if R/B# or RDY is ready.

Table 32: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	N_{VB}	1,998	2,048	Blocks	1

1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below N_{VB} during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Table 33: Array Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial page programs	—	2	Cycles	1, 2
tBERS	Erase Block operation time	3	10	ms	
tCBSY	Cache busy	3	500	µs	
tDBSY	Dummy busy time	0.5	1	µs	
tRCBSY	Cache read busy time	3	25	µs	
tFEAT	Busy time for SET FEATURES and GET FEATURES operations	—	1	µs	
tITC	Busy time for interface change	—	1	µs	3
tLPROG	LAST PAGE PROGRAM operation time	—	—	µs	4
tOBSY	Busy time for OTP Data Program operation if OTP is protected	—	30	µs	
tPOR	Power-on reset time	—	1	ms	
tPROG	Program Page operation time	160	500	µs	
tR	Read Page operation time (single-plane)	—	25	µs	
	Read Page operation time (multi-plane)	—	30	µs	

1. It is recommended that the host use an NOP of one except for the occasion where data stops within the middle of a page. Using NOP of 2 more than one time within the block increases the possibility of over-programming a page leading to potential program disturbs within the block.
2. The pages in the OTP Block have an NOP of 1.
3. tITC (max) is the busy time when the interface changes from asynchronous to synchronous using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the tITC time, any command, including READ STATUS (70h) and SELECT LUN WITH STATUS (78h), is prohibited.
4. tLPROG = tPROG (last page) + tPROG (last page – 1) – command load time (last page) – address load time (last page) – data load time (last page).

Timing Diagrams

Synchronous Interface

Figure 62: READ ID Operation

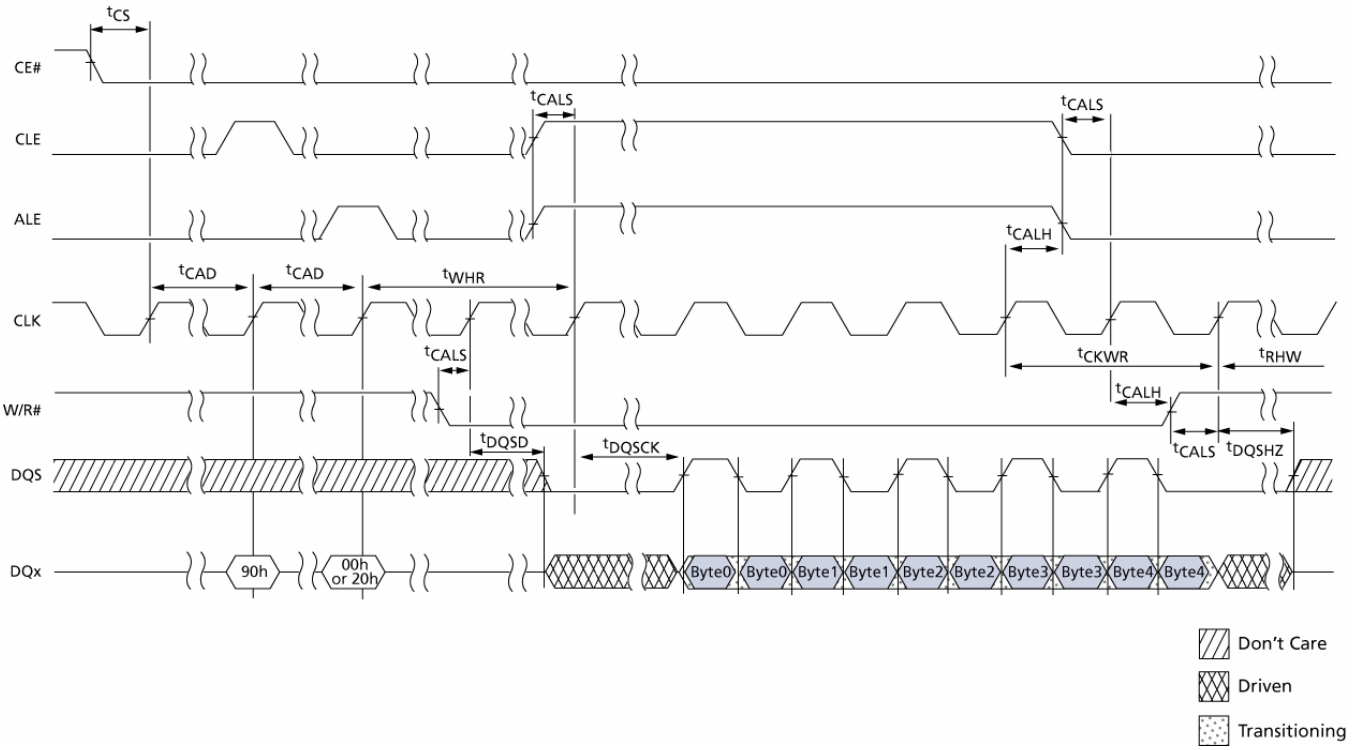


Figure 63: GET FEATURES Operation

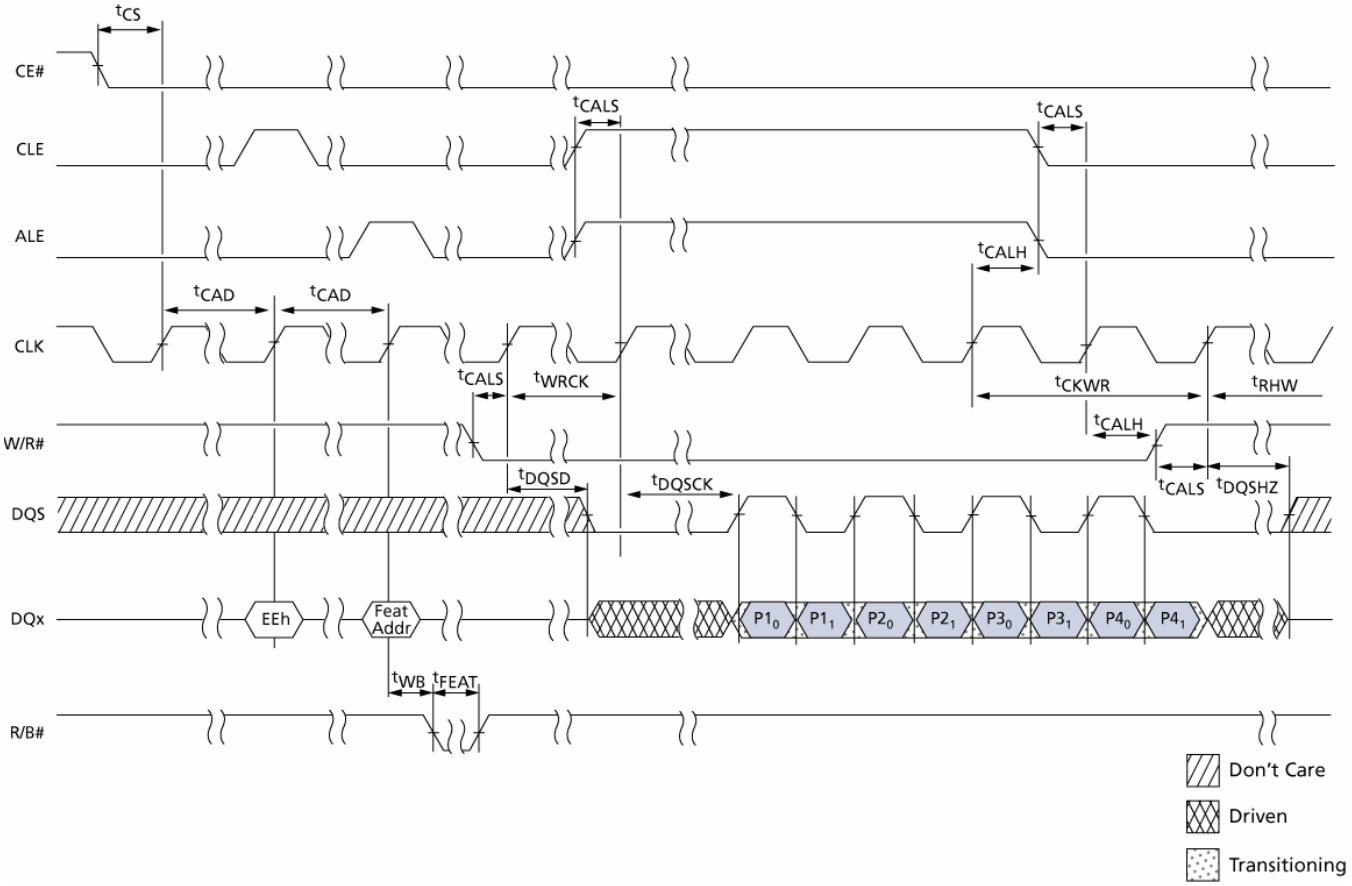


Figure 64: SET FEATURES Operation

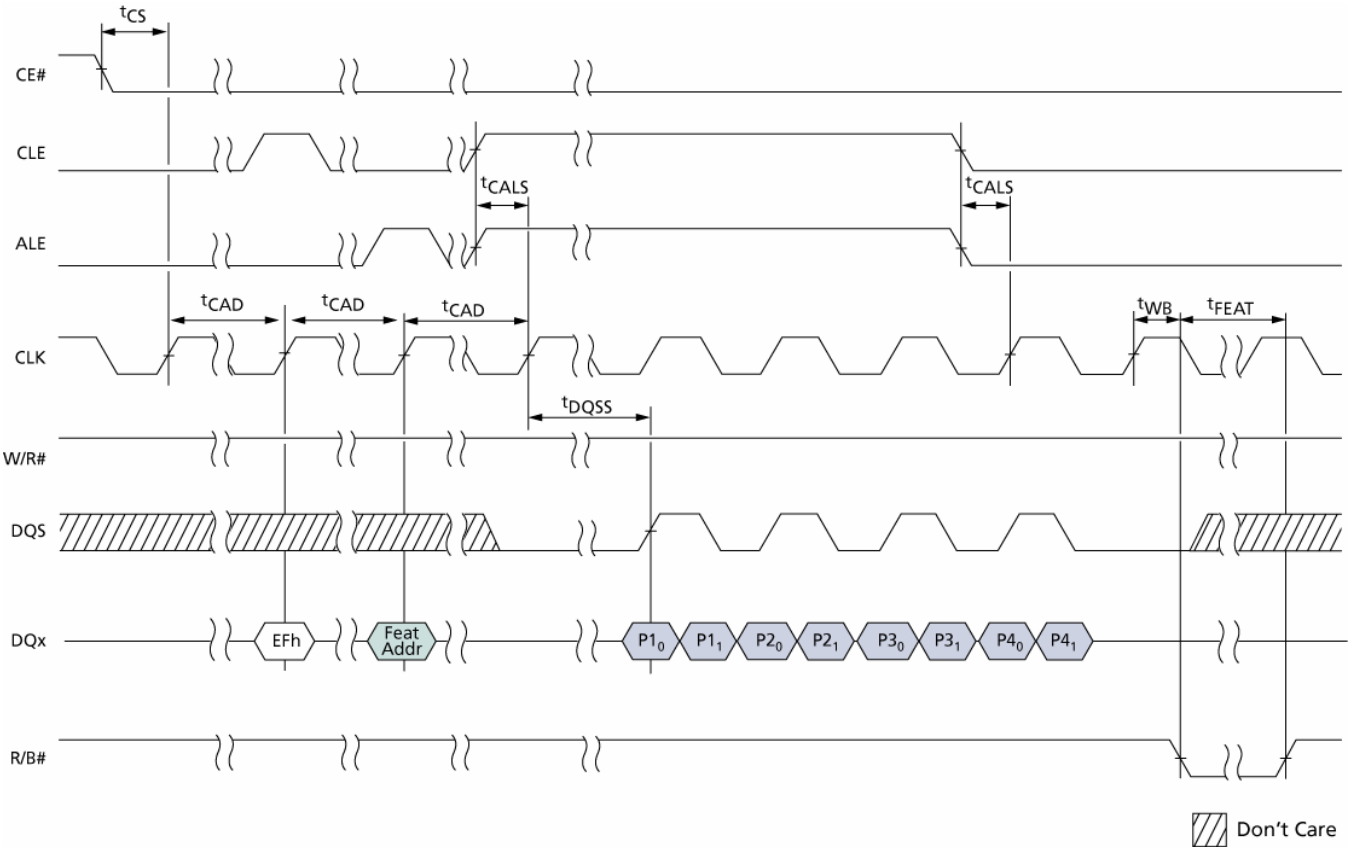


Figure 65: READ STATUS Cycle

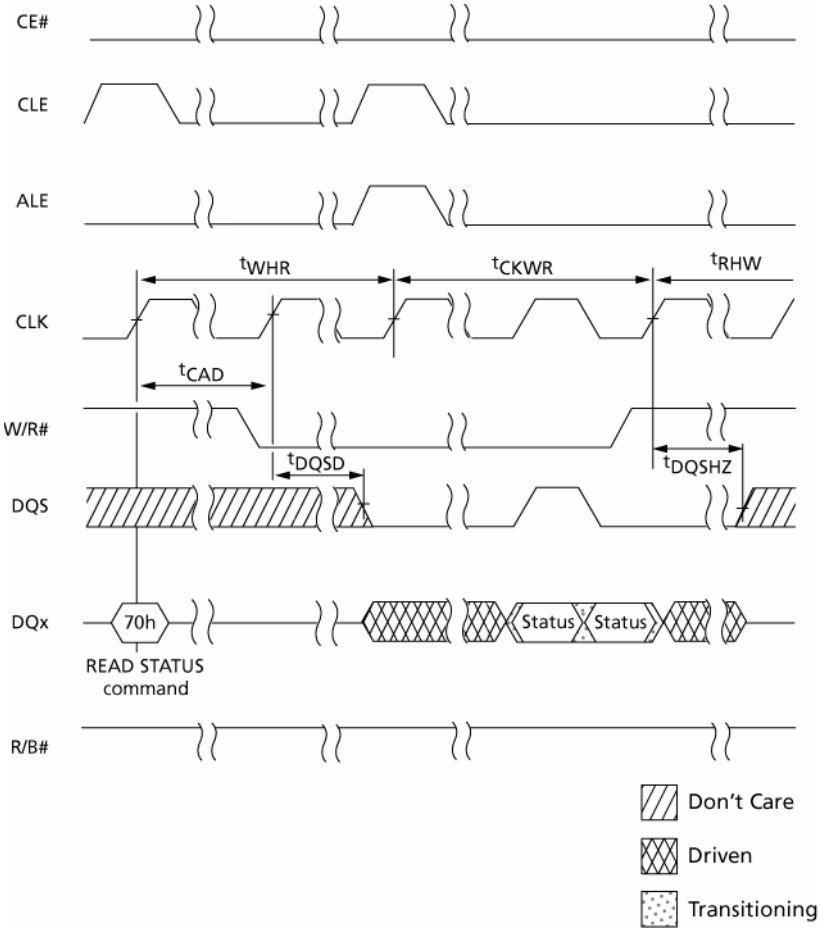


Figure 66: SELECT LUN with STATUS Operation

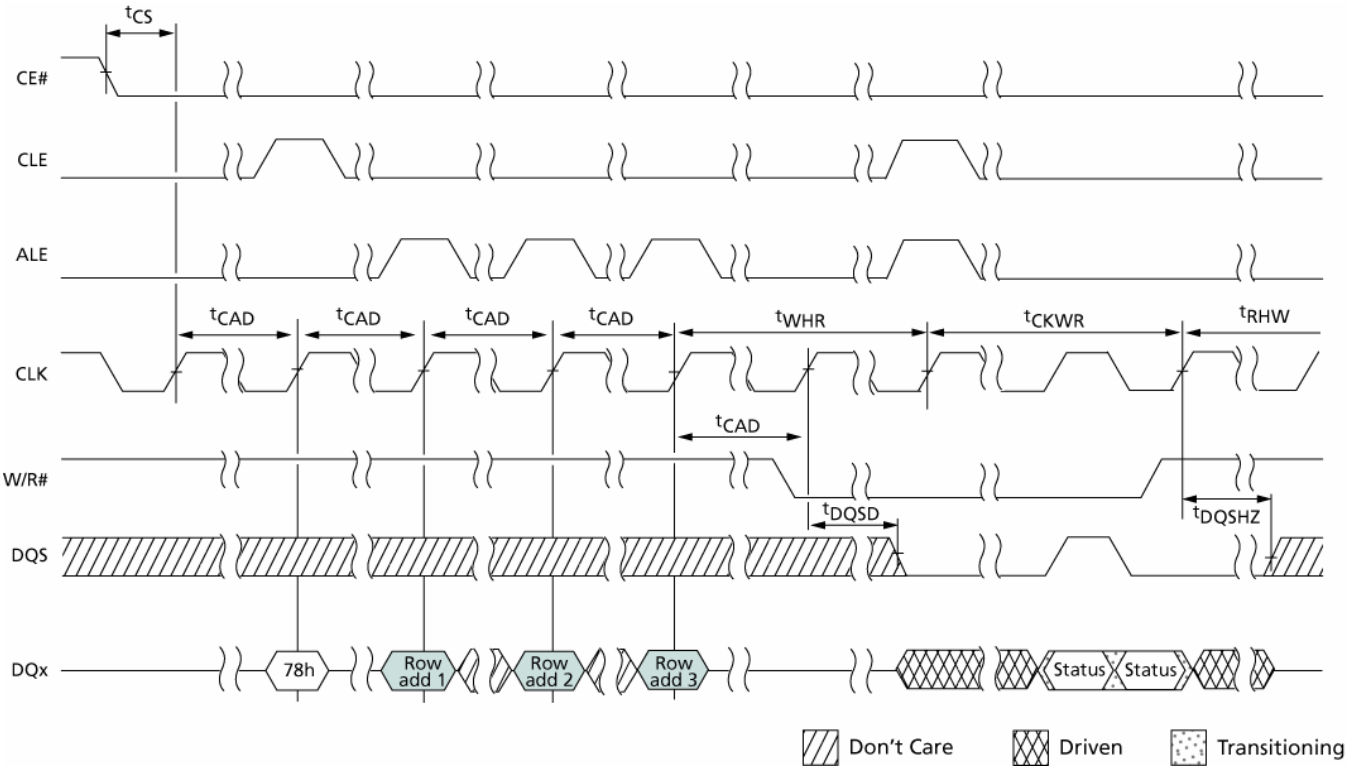


Figure 67: READ PARAMETER PAGE Operation

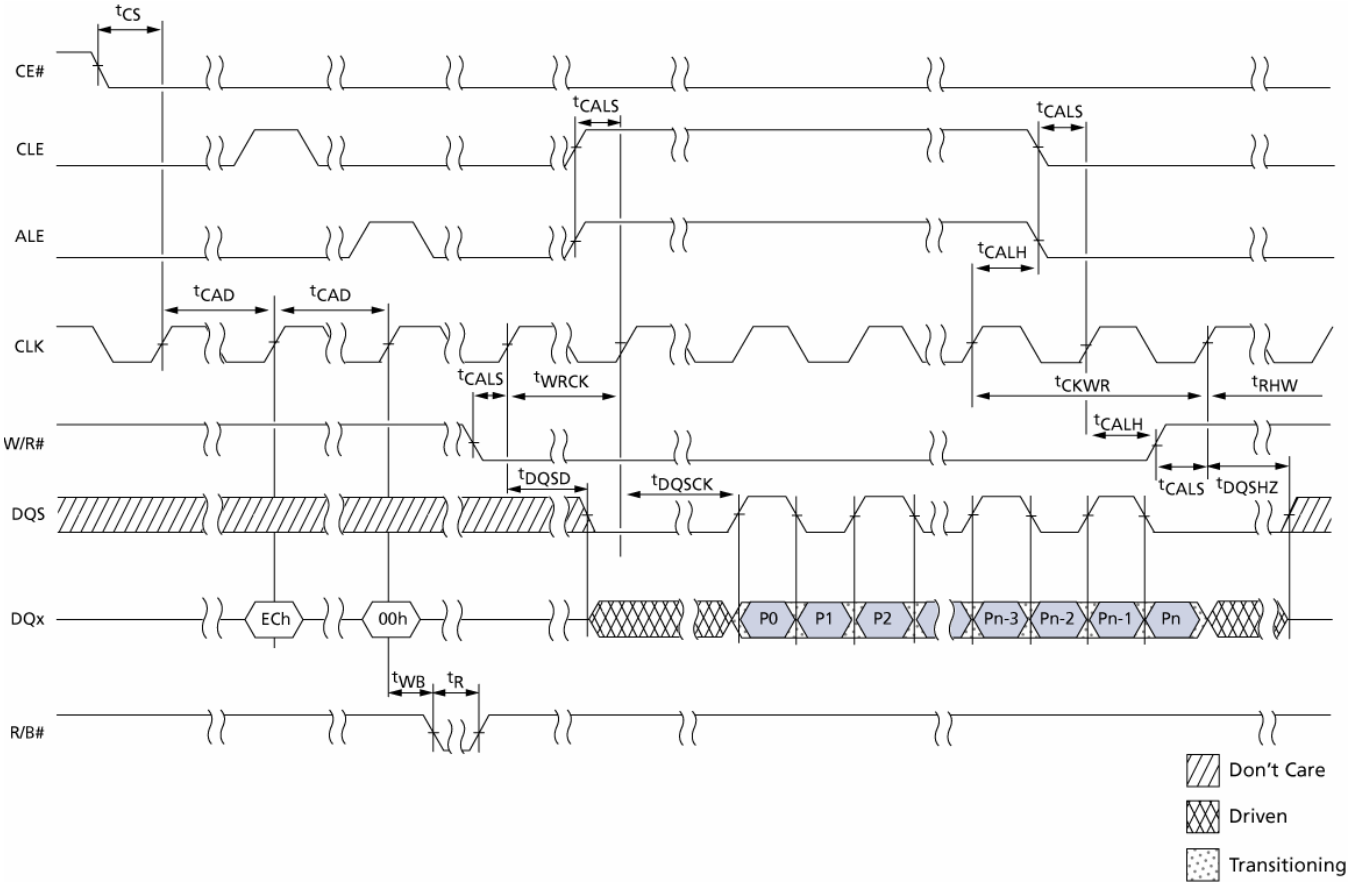


Figure 68: READ PAGE Operation

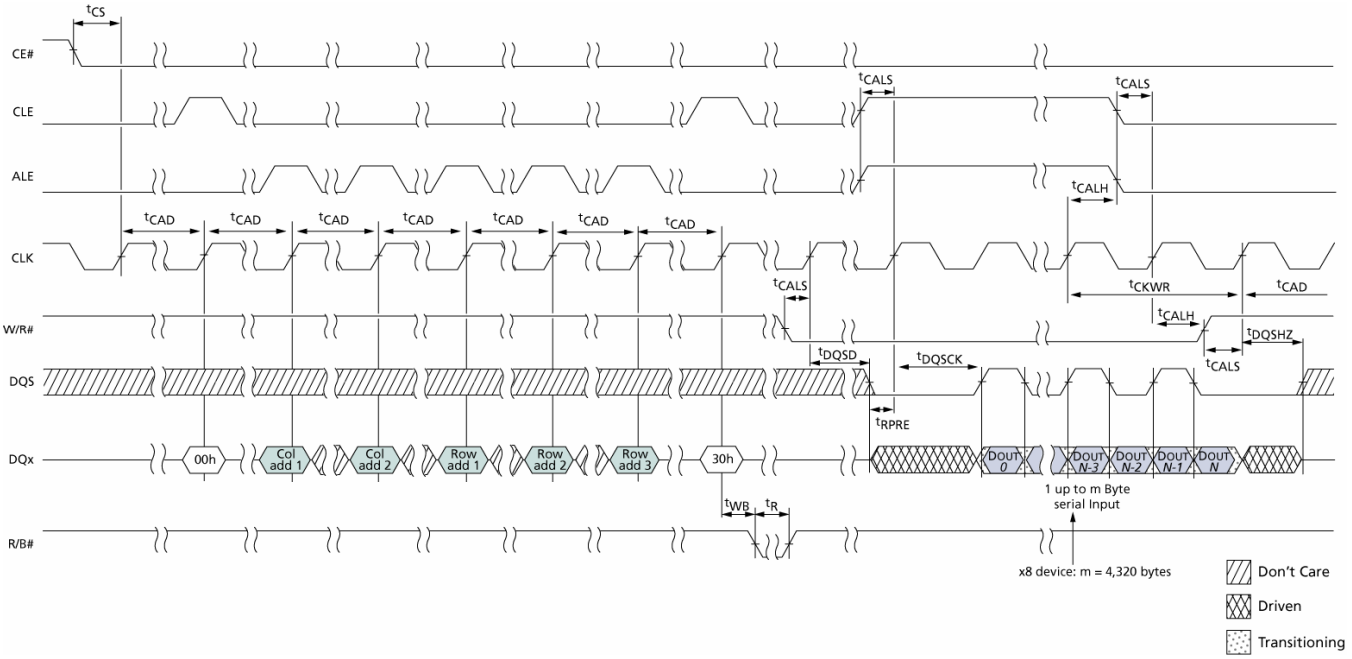


Figure 69: CHANGE READ COLUMN

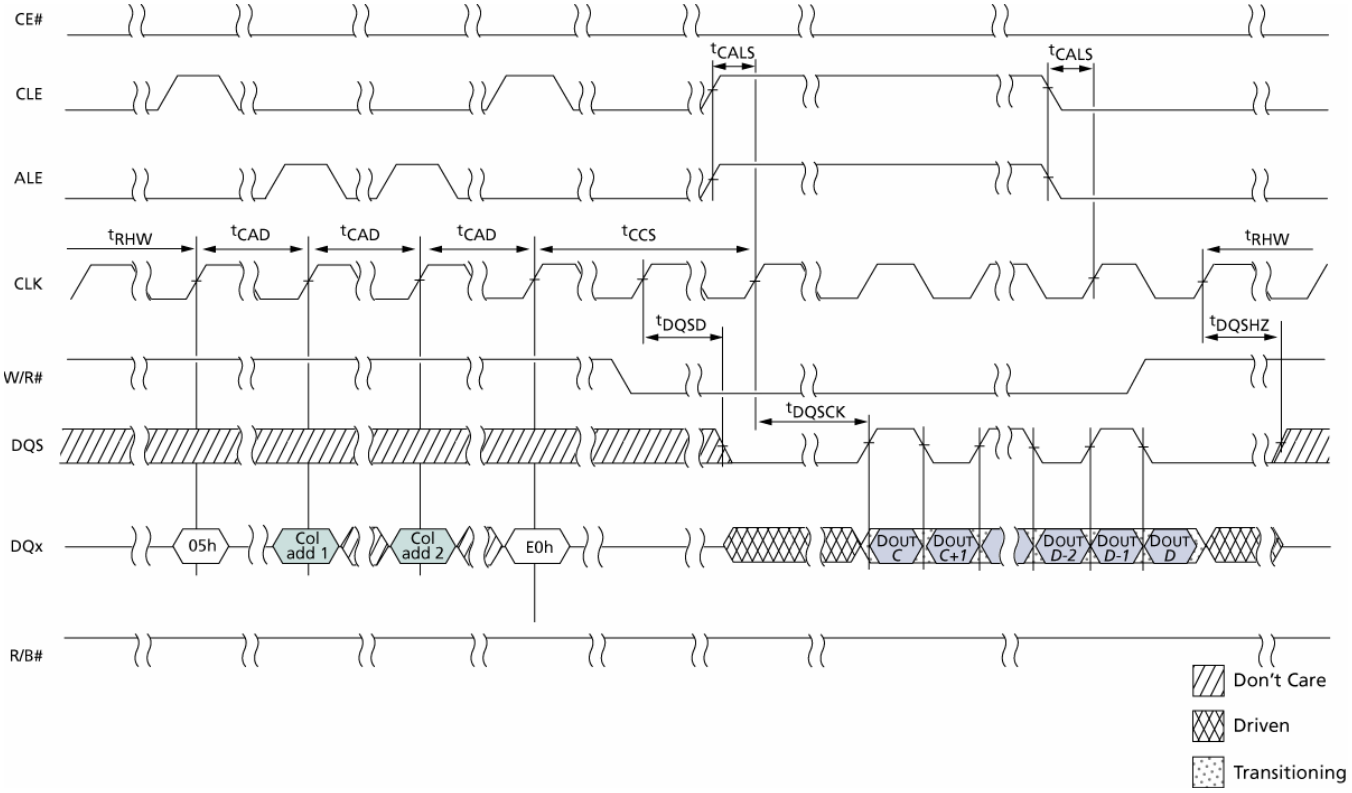


Figure 70: READ PAGE CACHE SEQUENTIAL

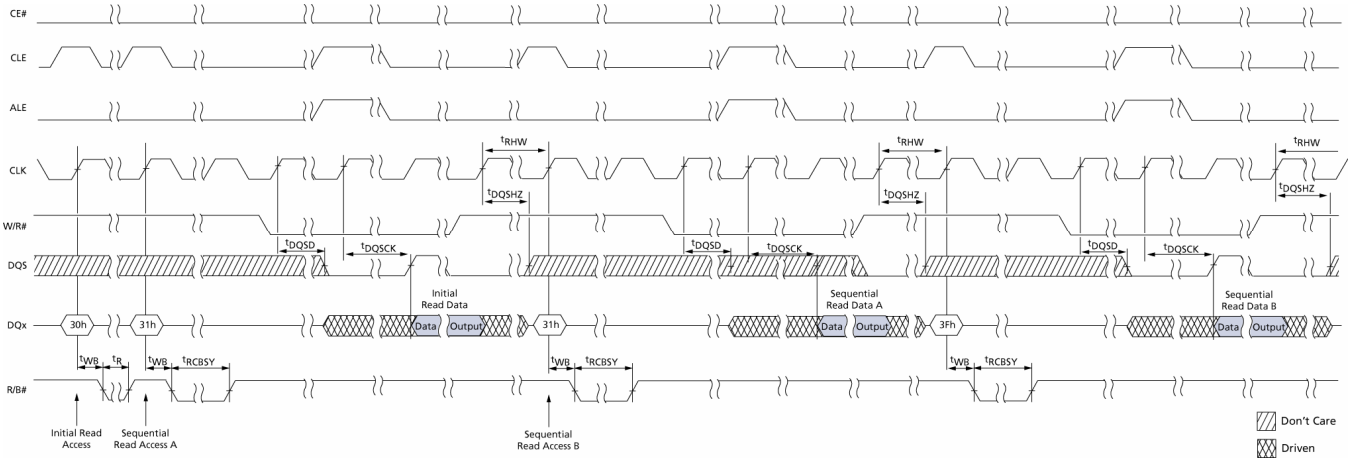


Figure 71: READ PAGE CACHE RANDOM

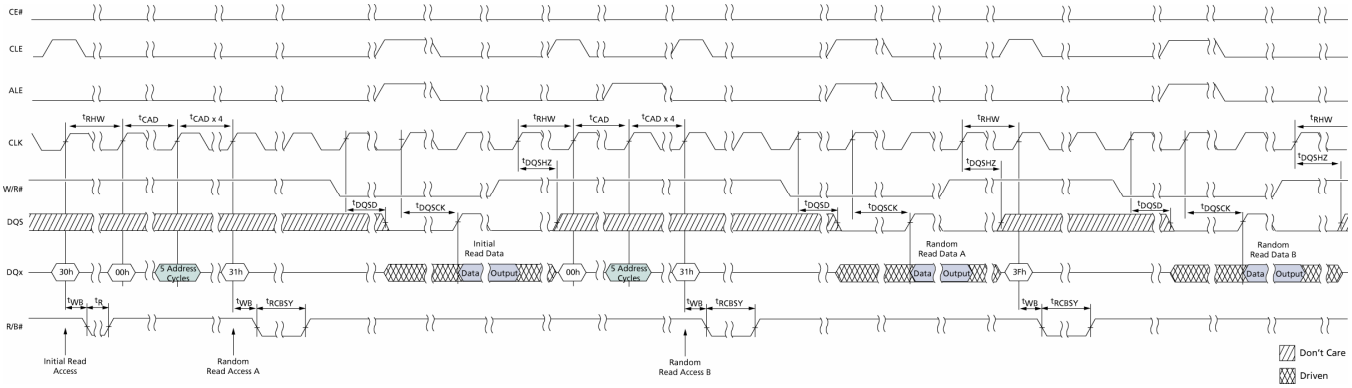


Figure 72: Multi-Plane Read Page (Four-plane Example) 1 of 2

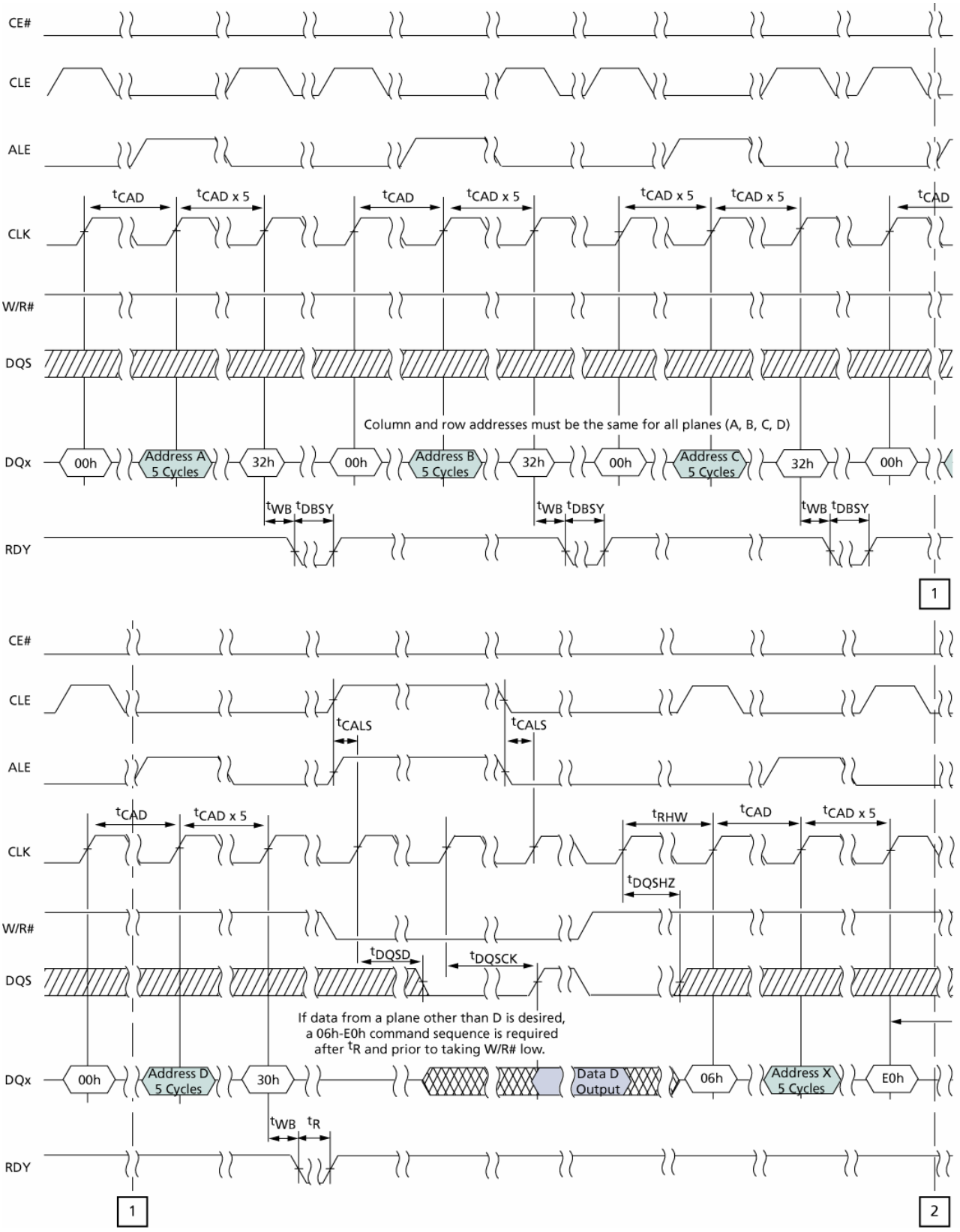


Figure 73: Multi-Plane Read Page (Four-plane Example) 2 of 2

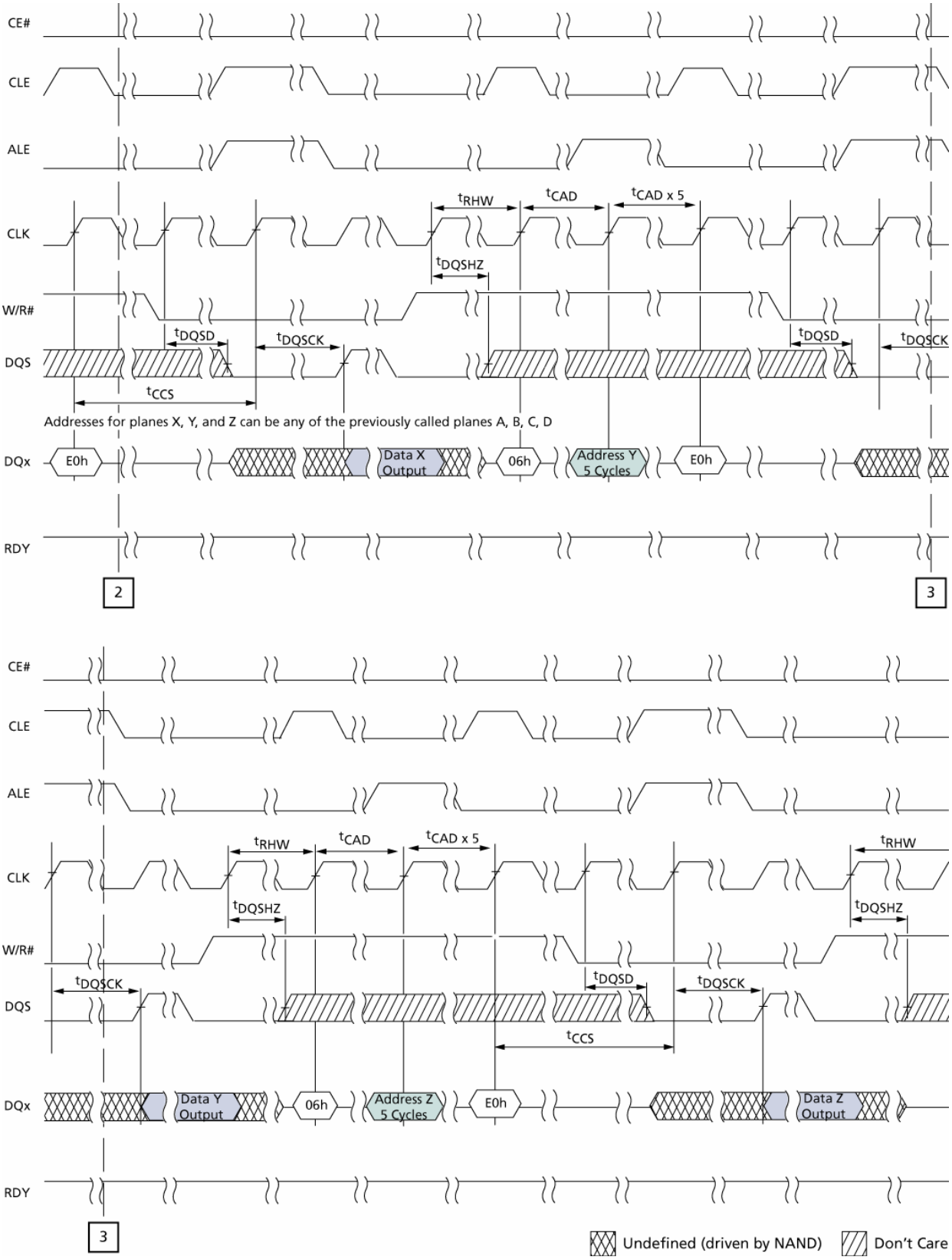


Figure 74: PROGRAM PAGE Operation

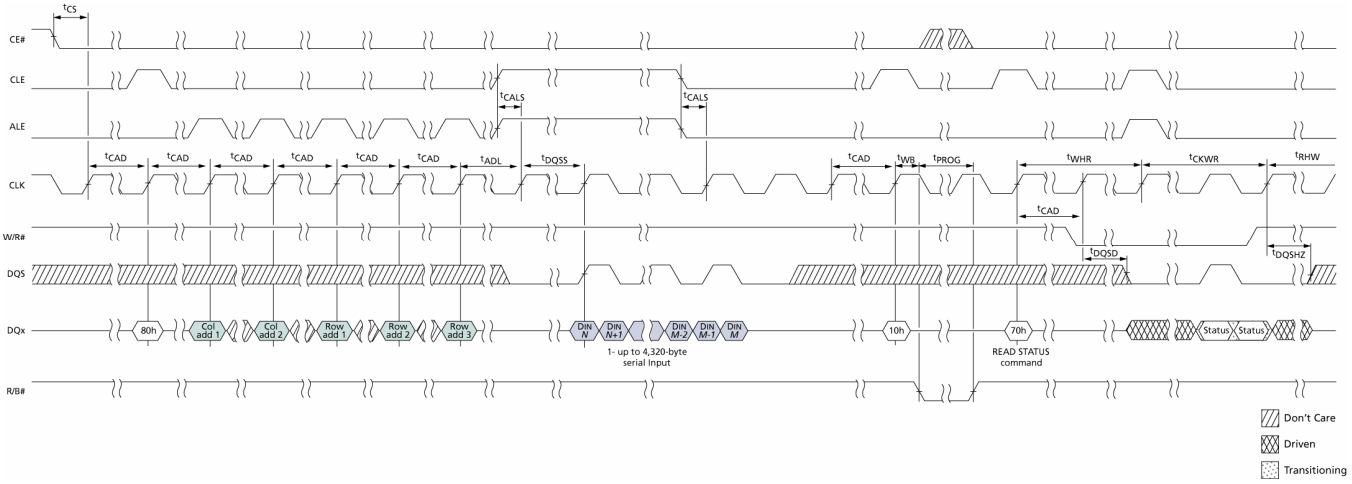


Figure 75: CHANGE WRITE COLUMN

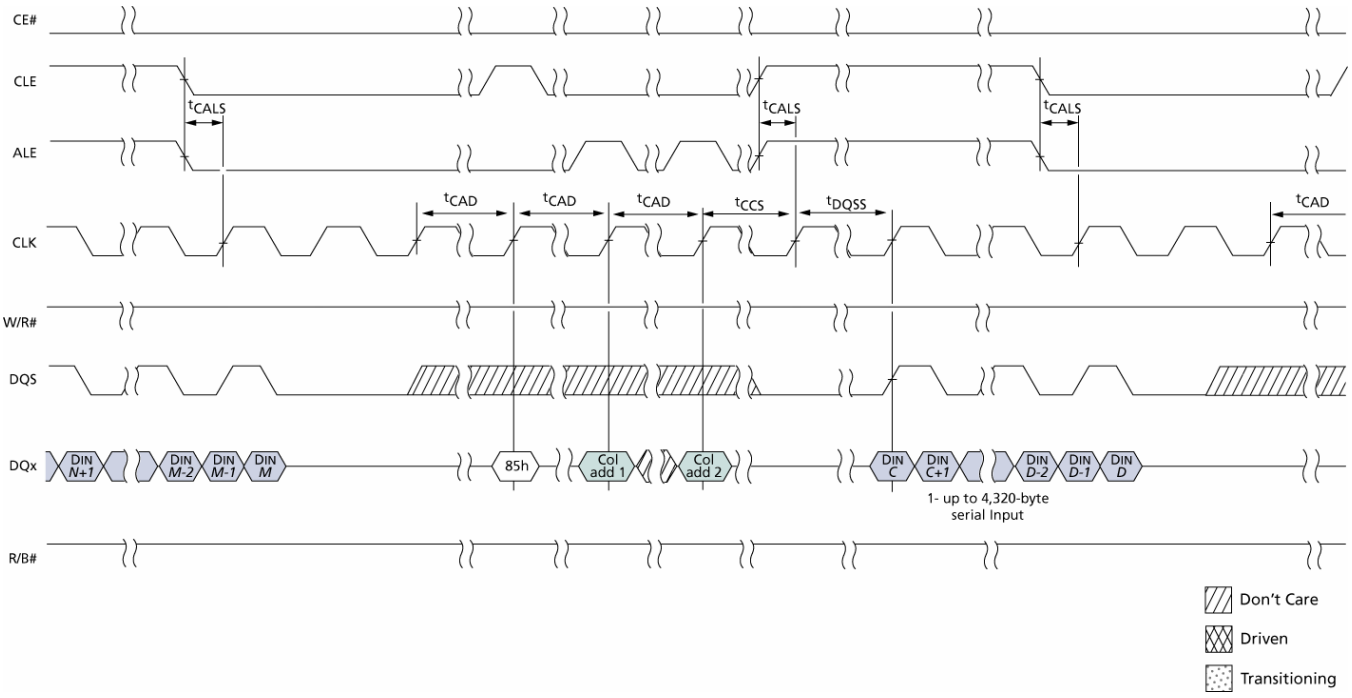


Figure 76: Multi-Plane Program Page (Four-plane Example) 1 of 2

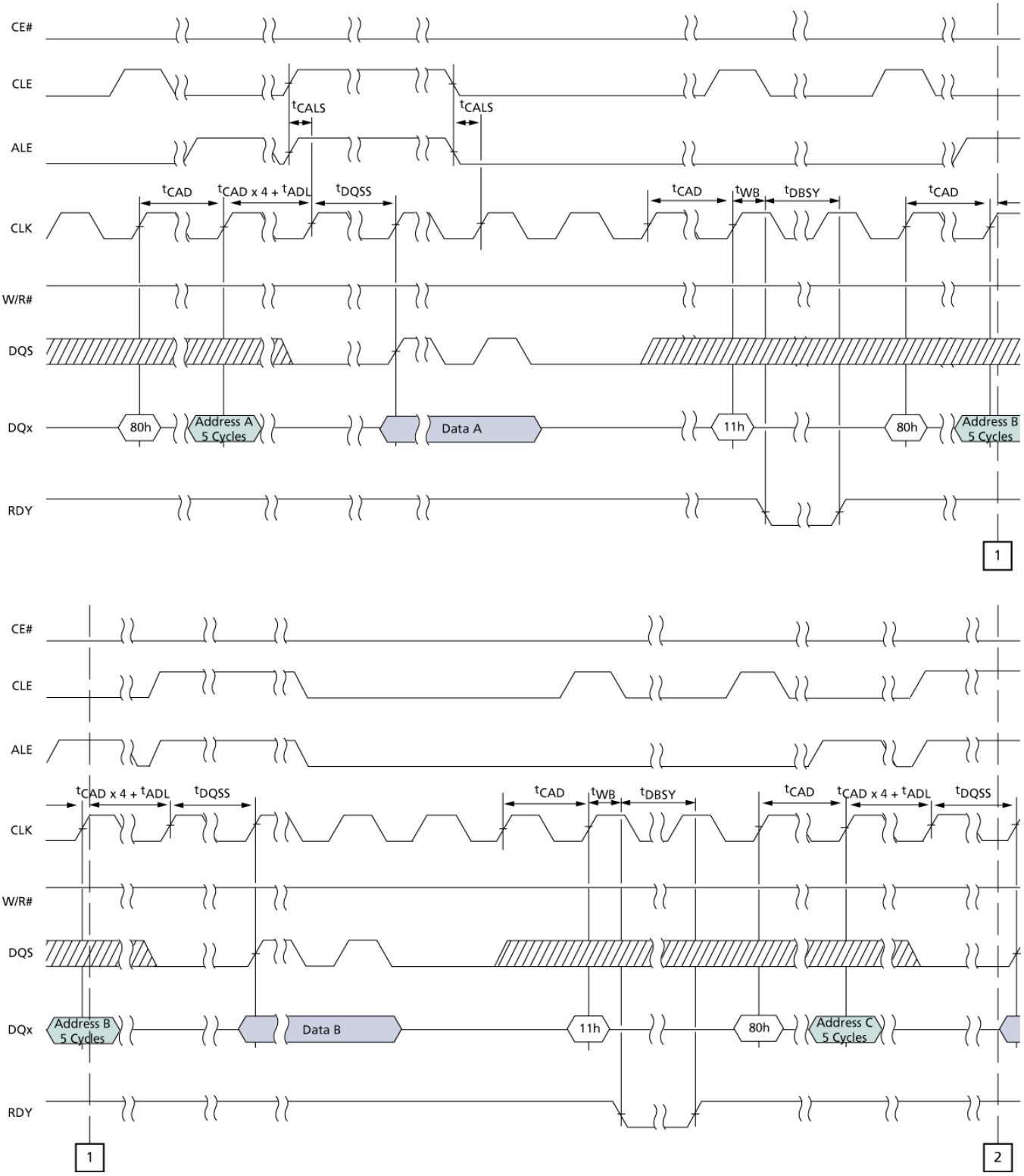


Figure 77: Multi-Plane Program Page (Four-plane Example) 2 of 2

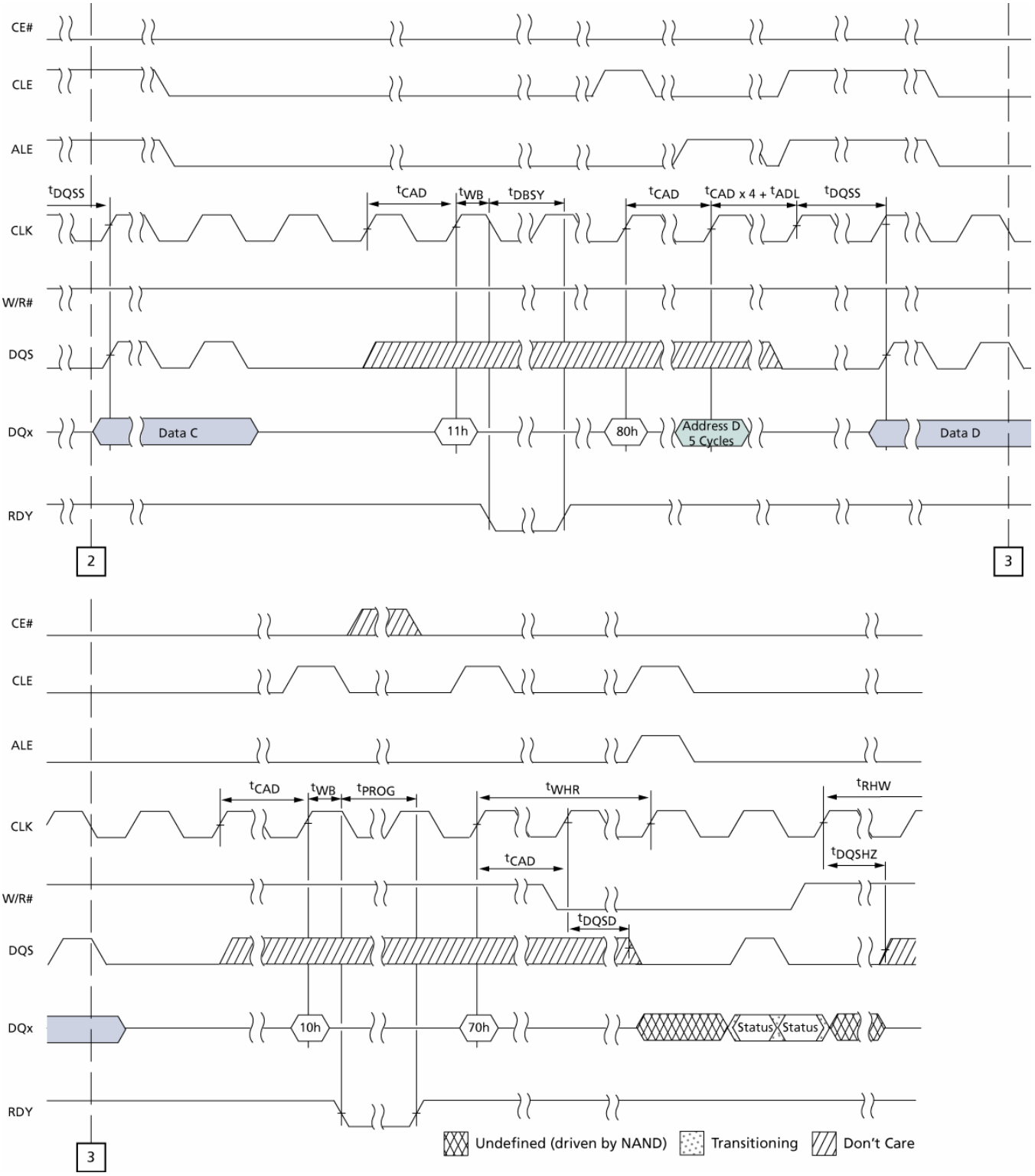


Figure 78: ERASE BLOCK

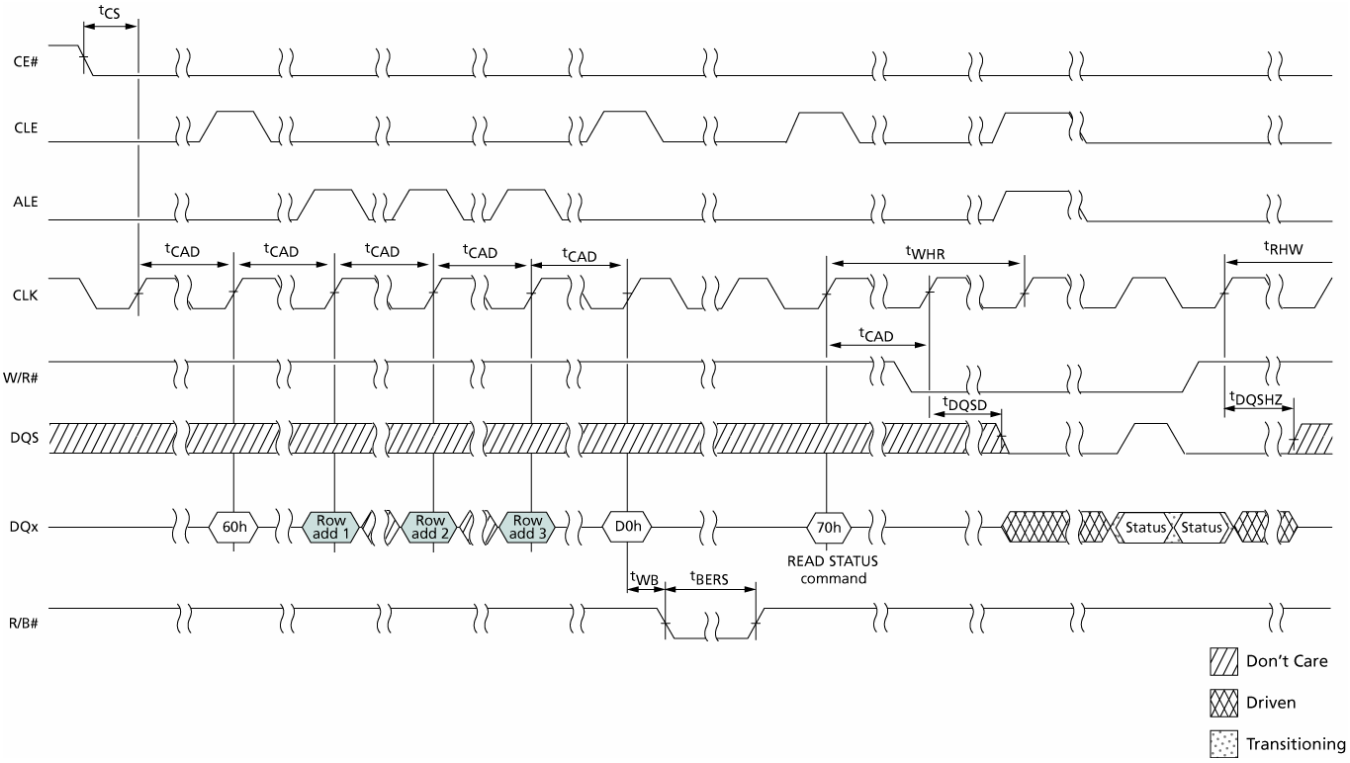


Figure 79: COPYBACK 1 of 2

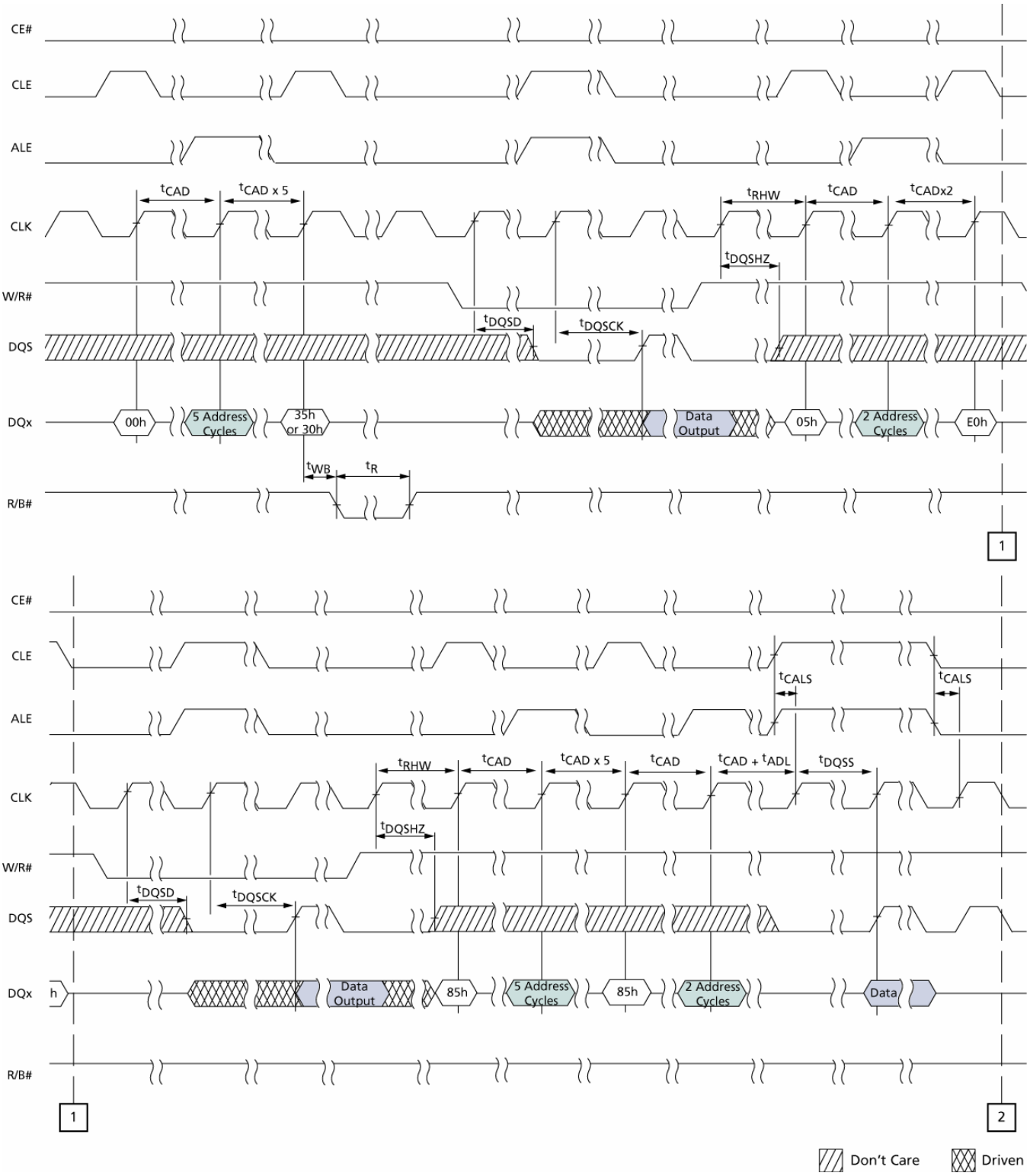


Figure 80: COPYBACK 2 of 2

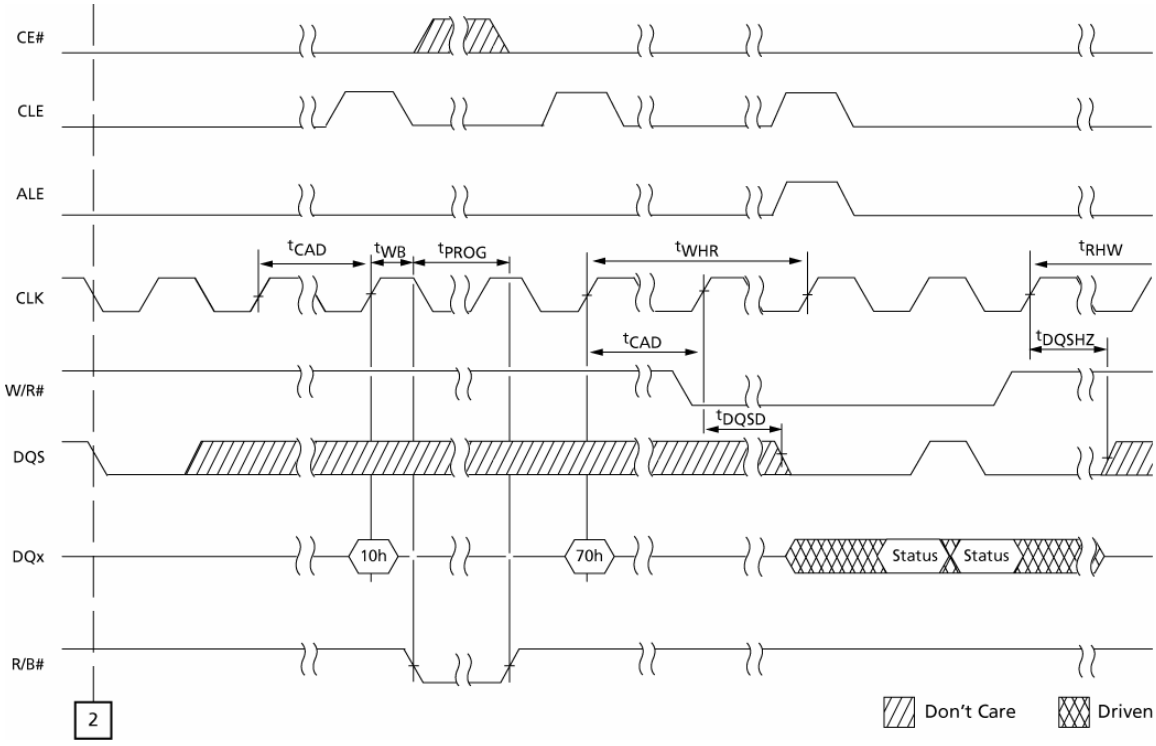


Figure 81: READ OTP PAGE

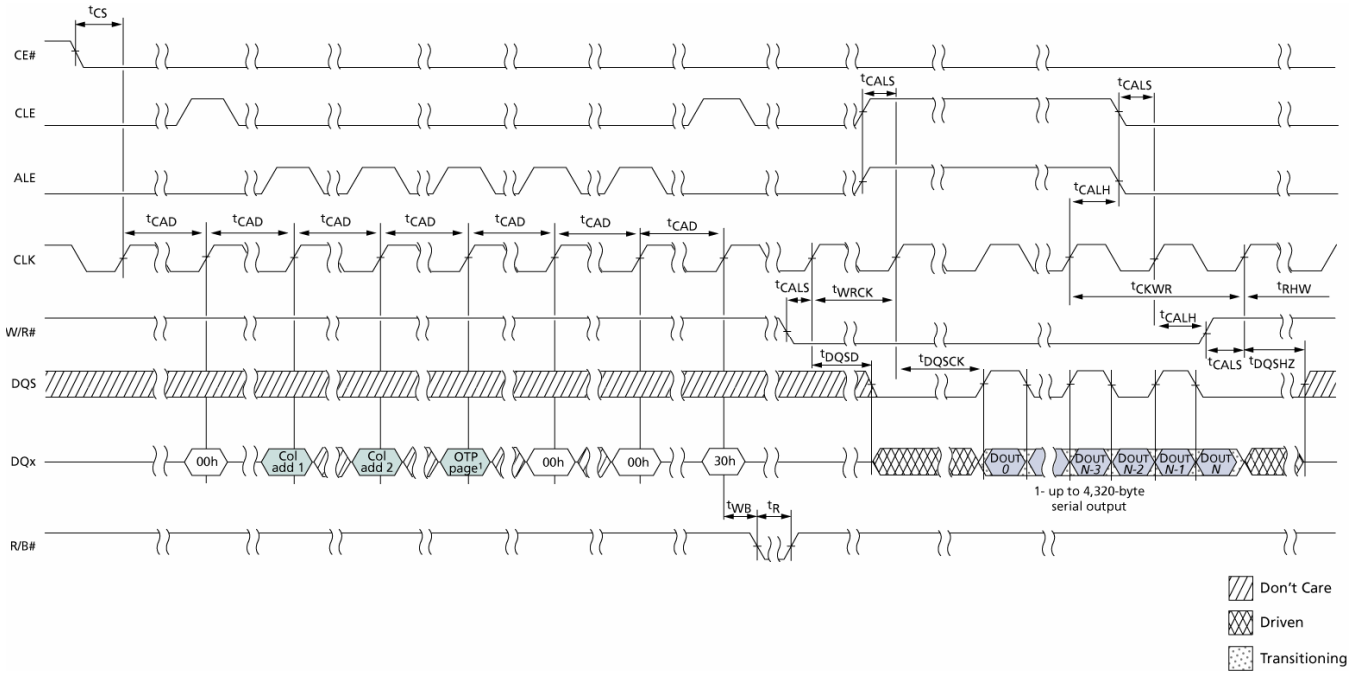


Figure 82: PROGRAM OTP PAGE

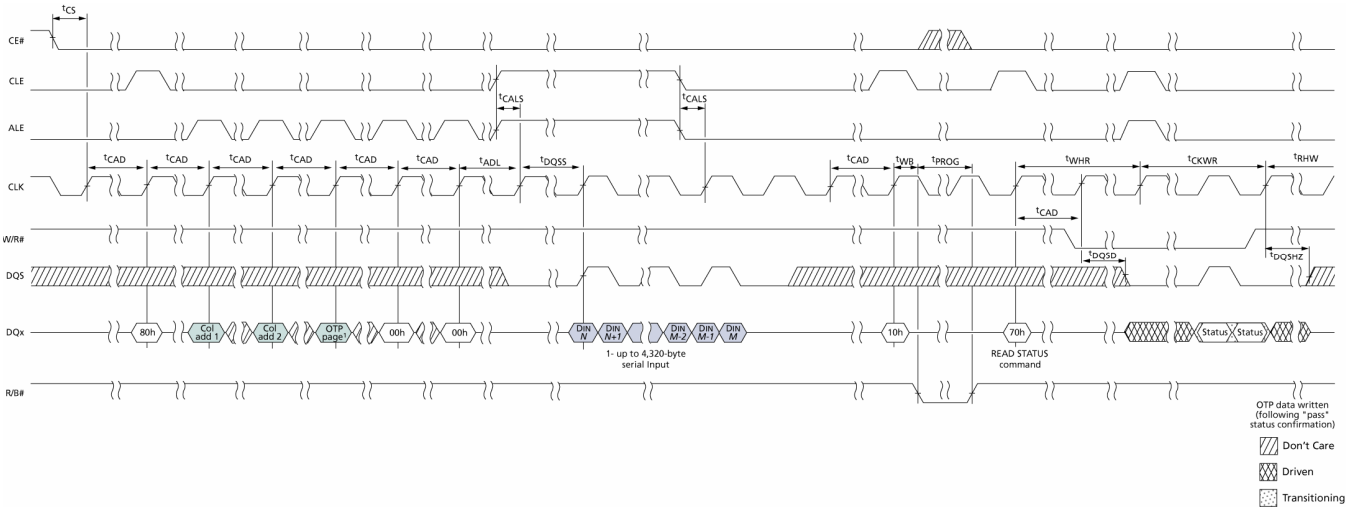
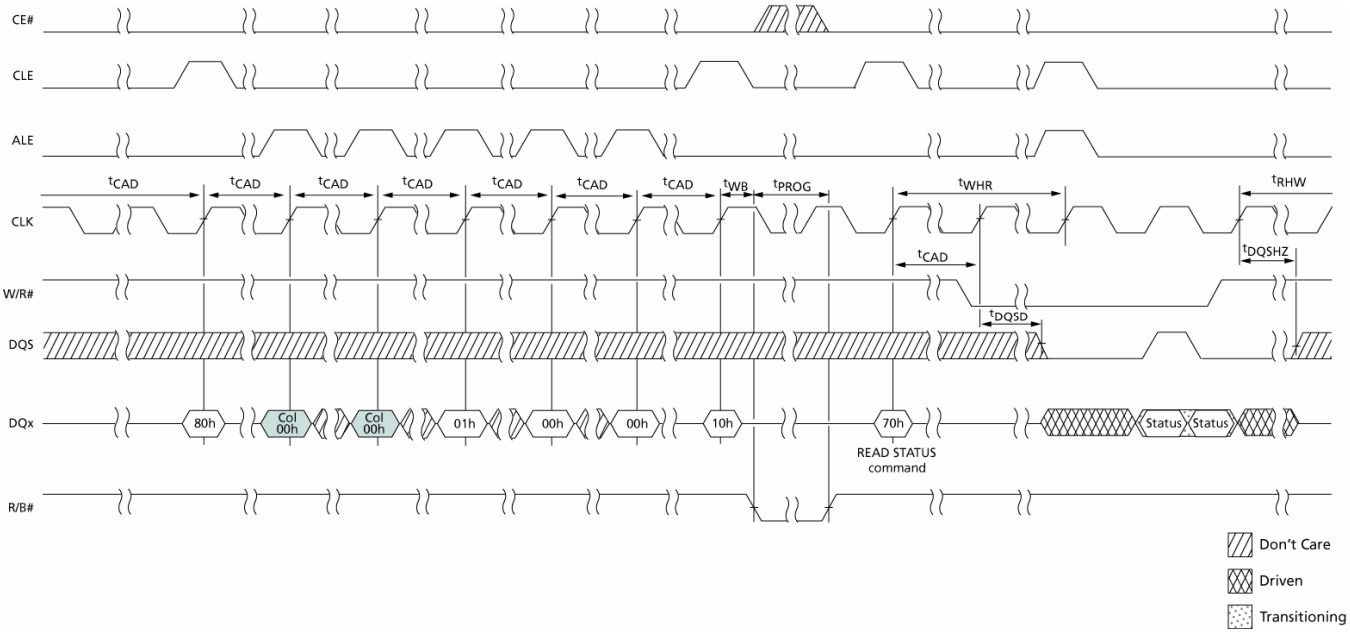


Figure 83: PROTECT OTP AREA



Asynchronous Interface

Figure 84: RESET Operation

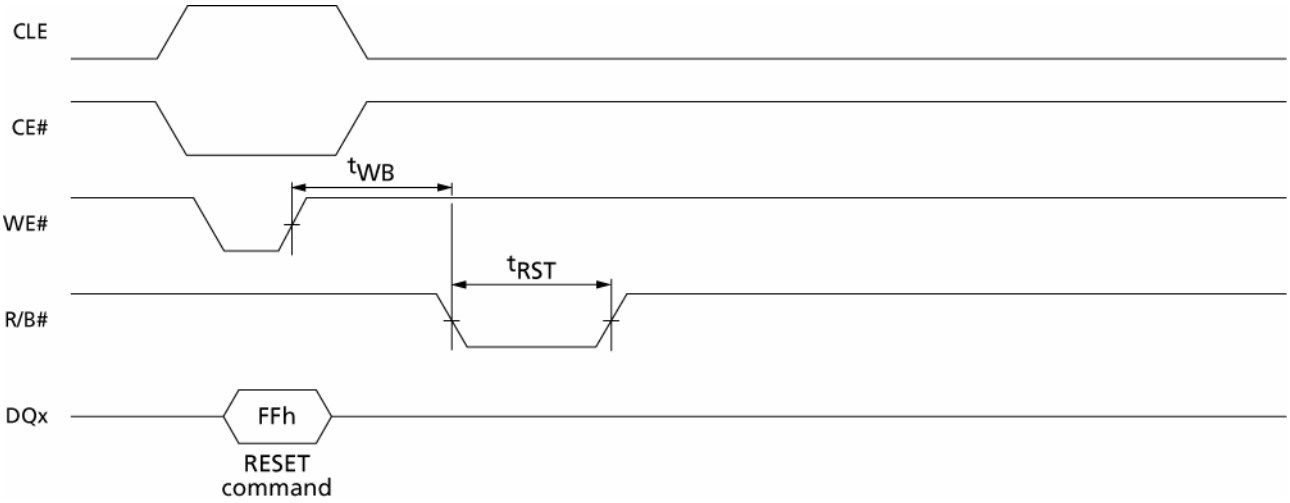


Figure 85: READ STATUS Cycle

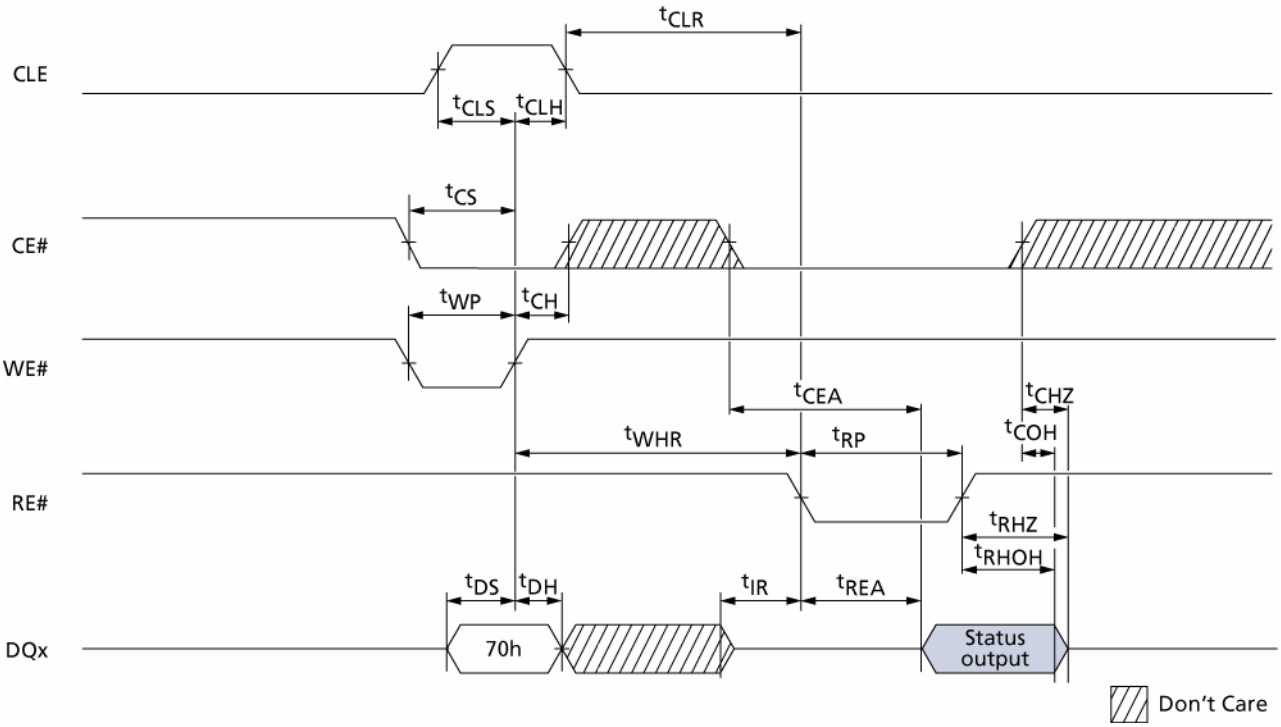


Figure 86: SELECT LUN WITH STATUS Cycle

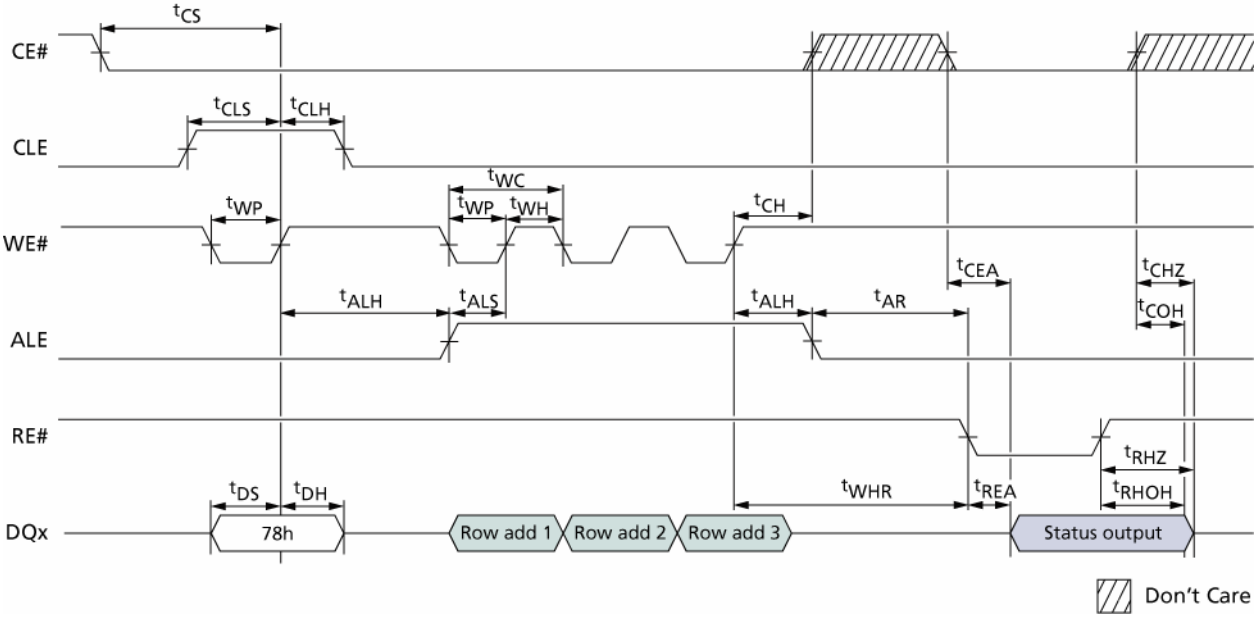


Figure 87: READ PARAMETER PAGE

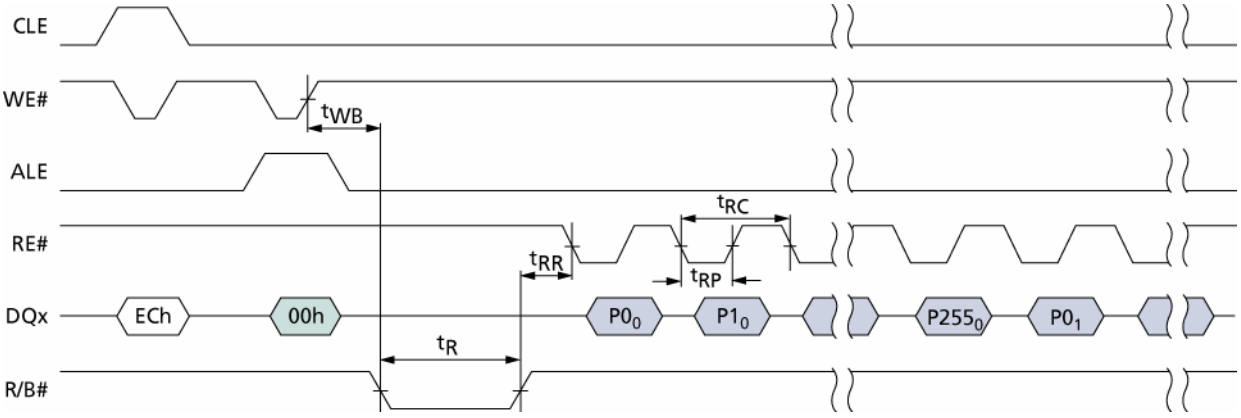


Figure 88: READ PAGE

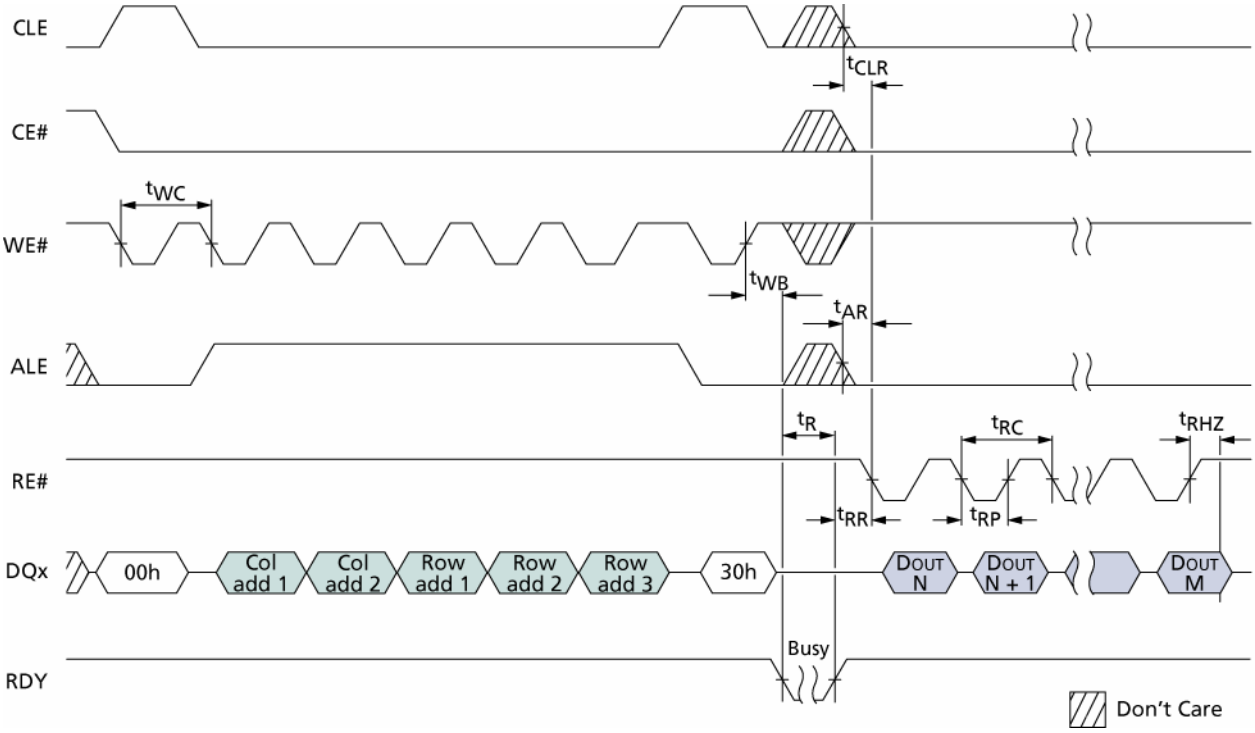


Figure 89: READ PAGE Operation with CE# "Don't Care"

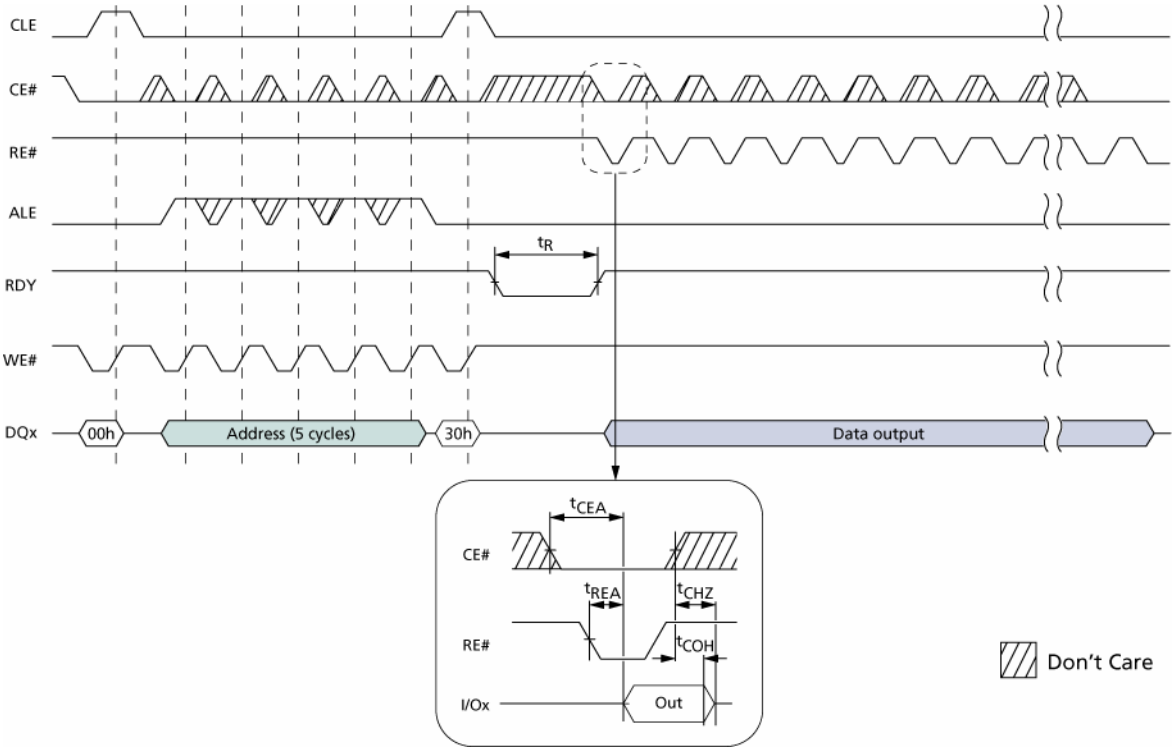


Figure 90: CHANGE READ COLUMN

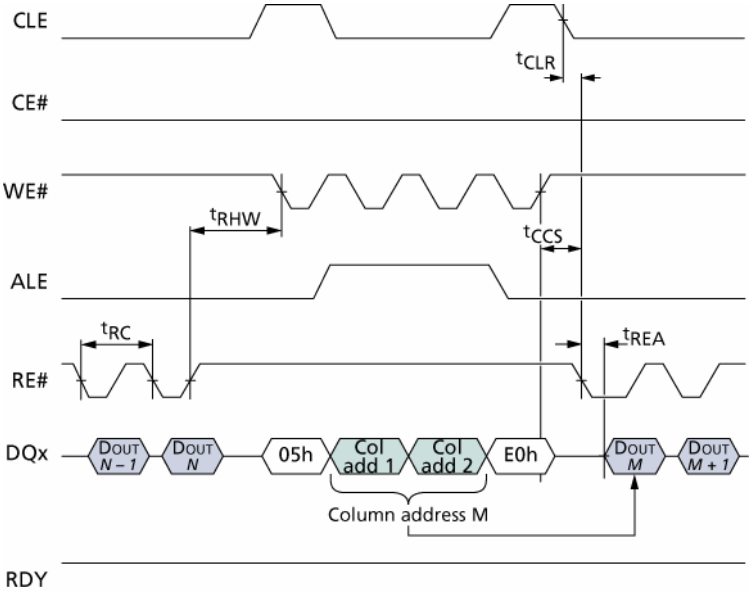


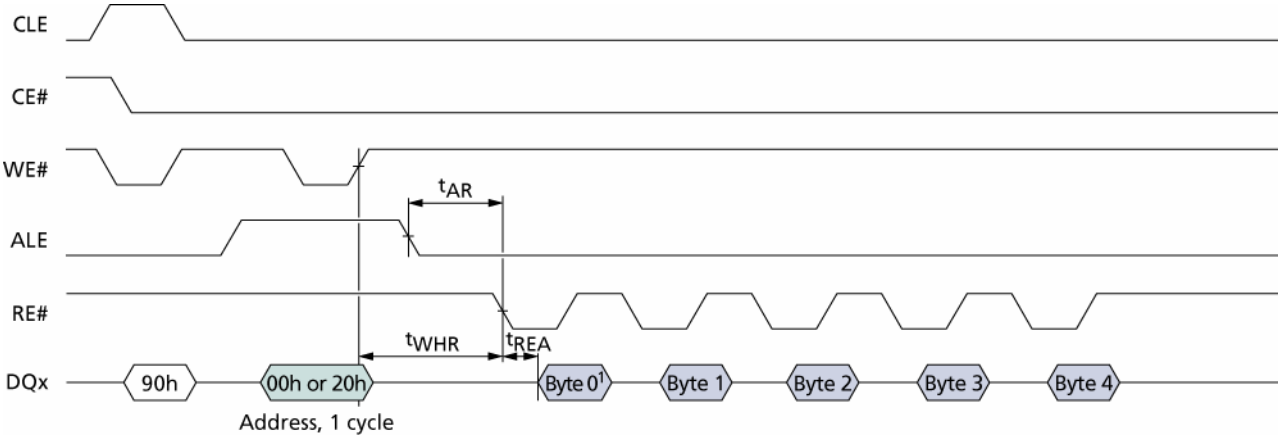
Figure 91: READ PAGE CACHE SEQUENTIAL

To do: To be added.

Figure 92: READ PAGE CACHE RANDOM

To do: To be added.

Figure 93: READ ID Operation



1. See Table 6 and Table 7 beginning on page 39 for byte definitions.

Figure 94: PROGRAM PAGE Operation

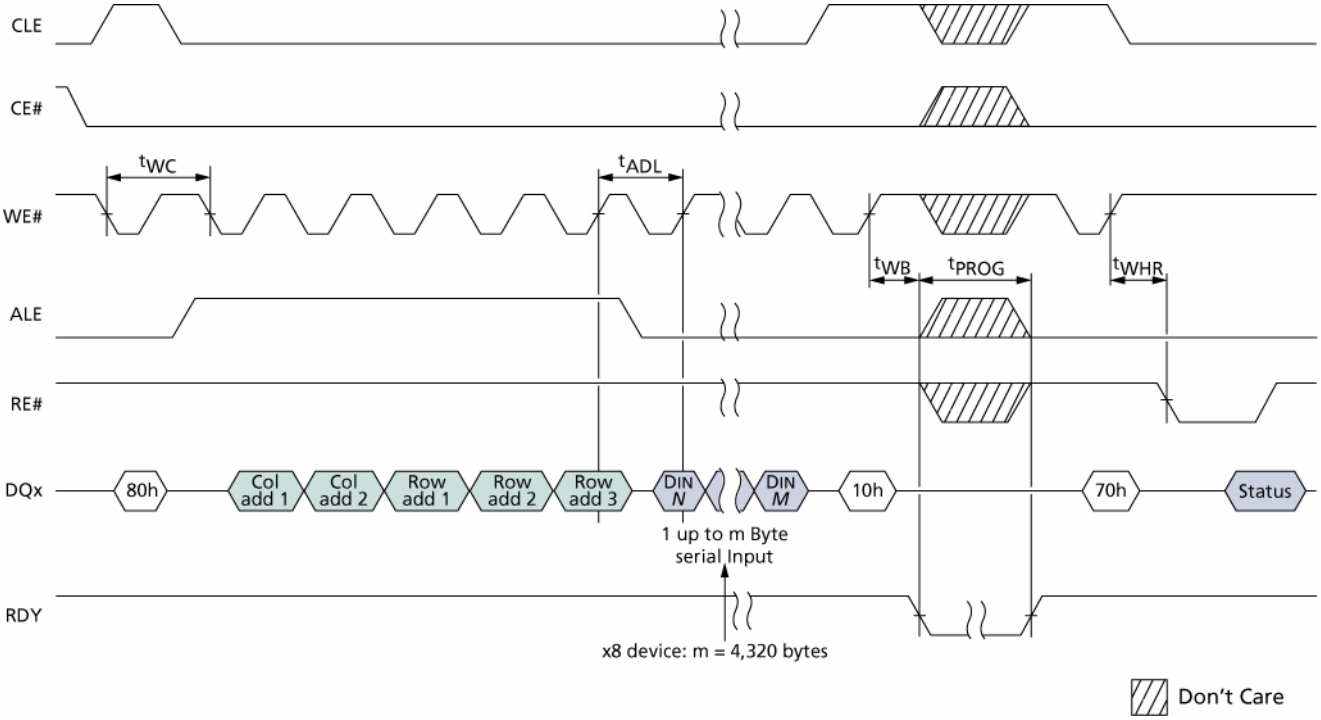


Figure 95: PROGRAM PAGE Operation with CE# "Don't Care"

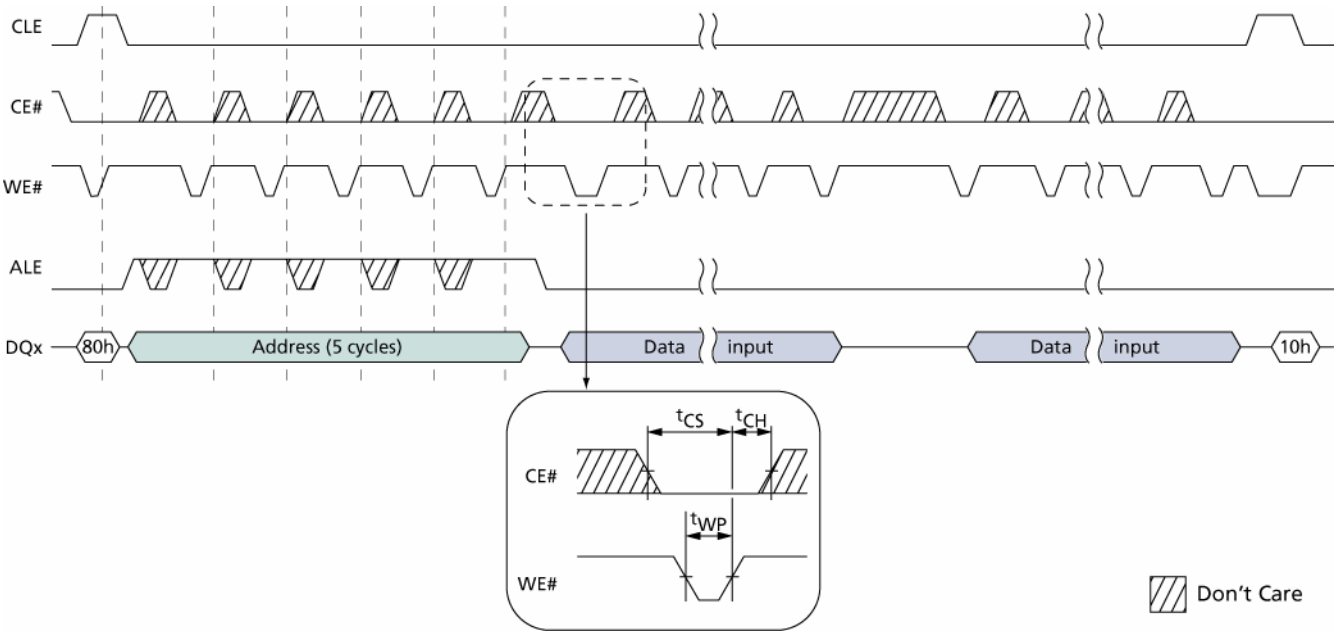


Figure 96: PROGRAM PAGE Operation with CHANGE WRITE COLUMN

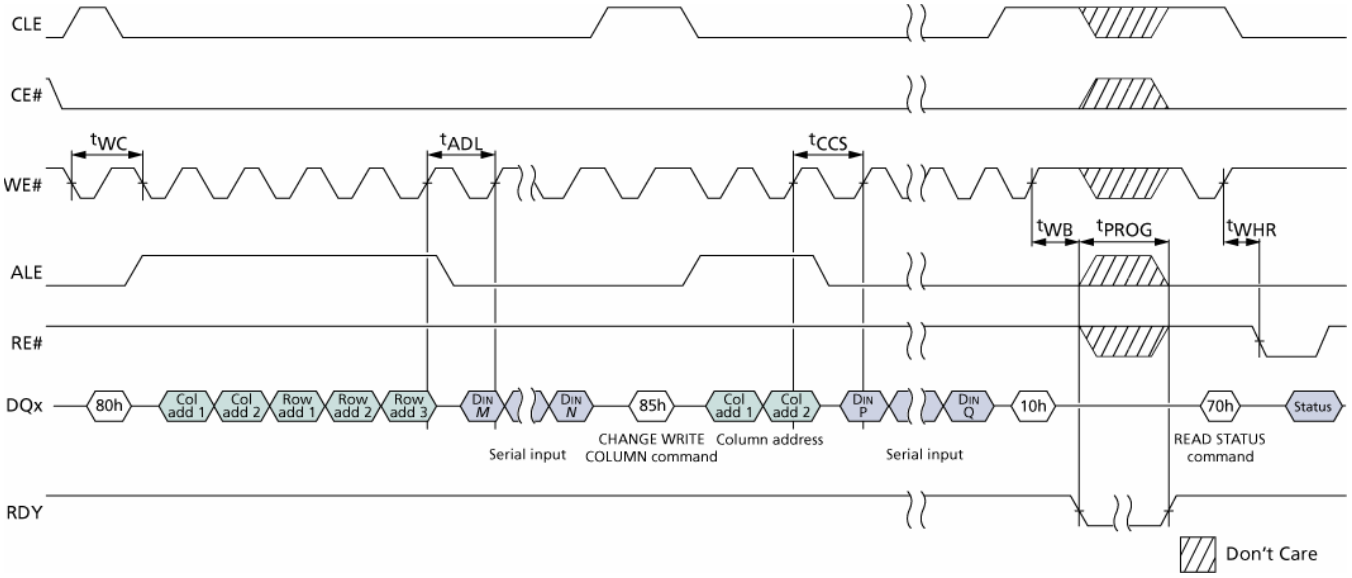


Figure 97: PROGRAM PAGE CACHE

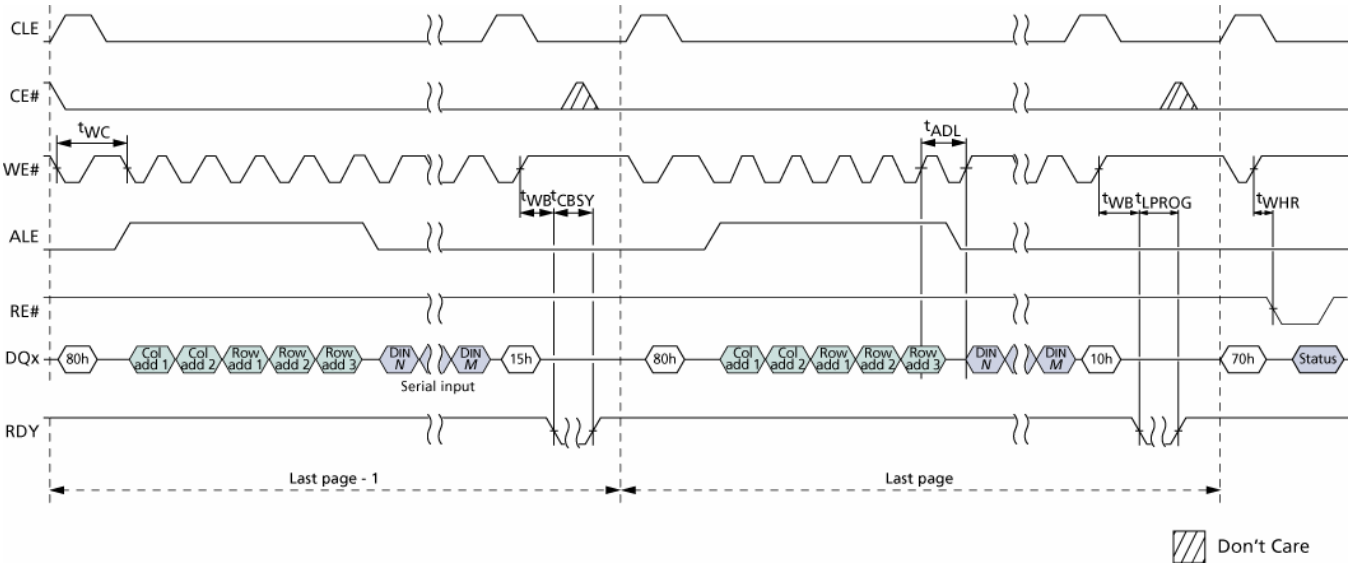


Figure 98: PROGRAM PAGE CACHE Ending on 15h

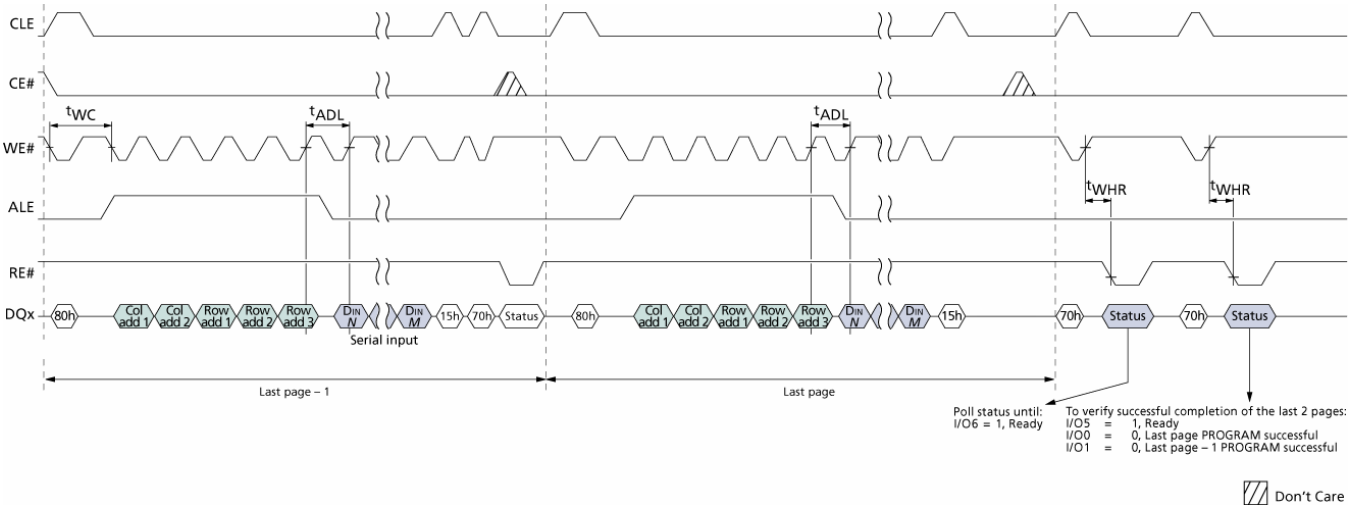


Figure 99: COPYBACK

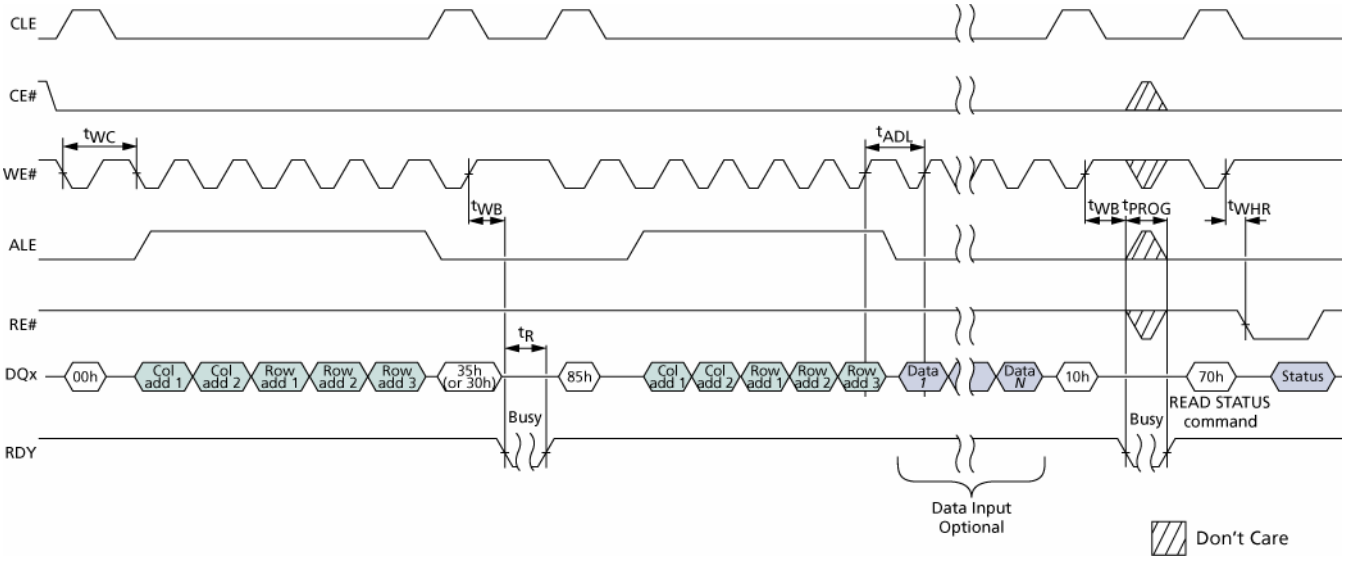
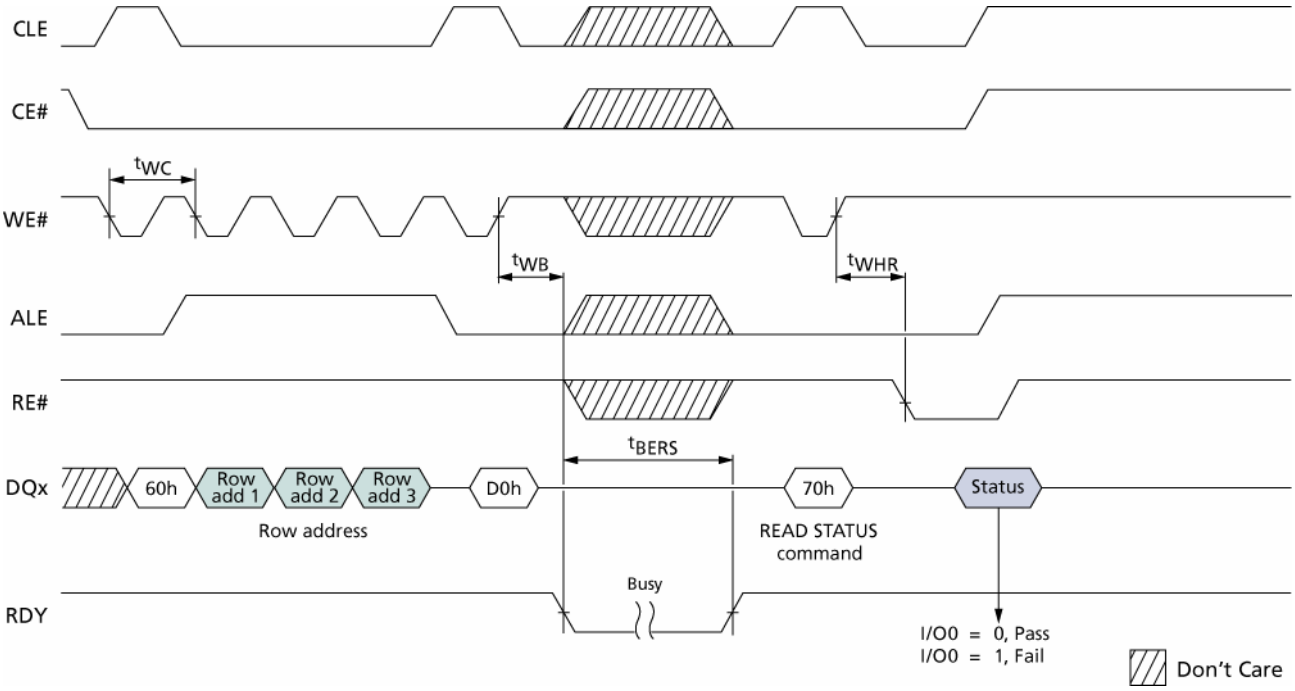
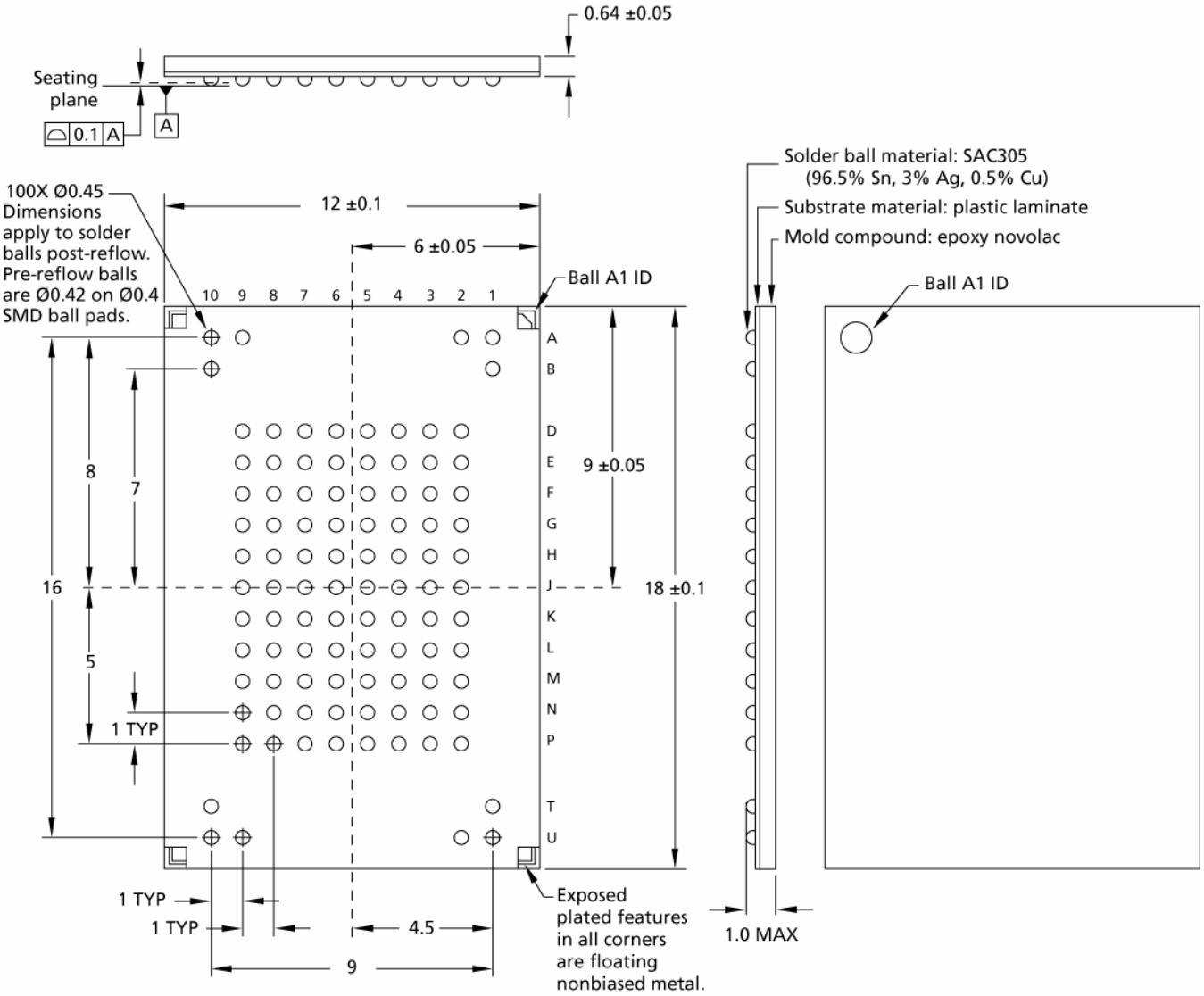


Figure 100: ERASE BLOCK Operation



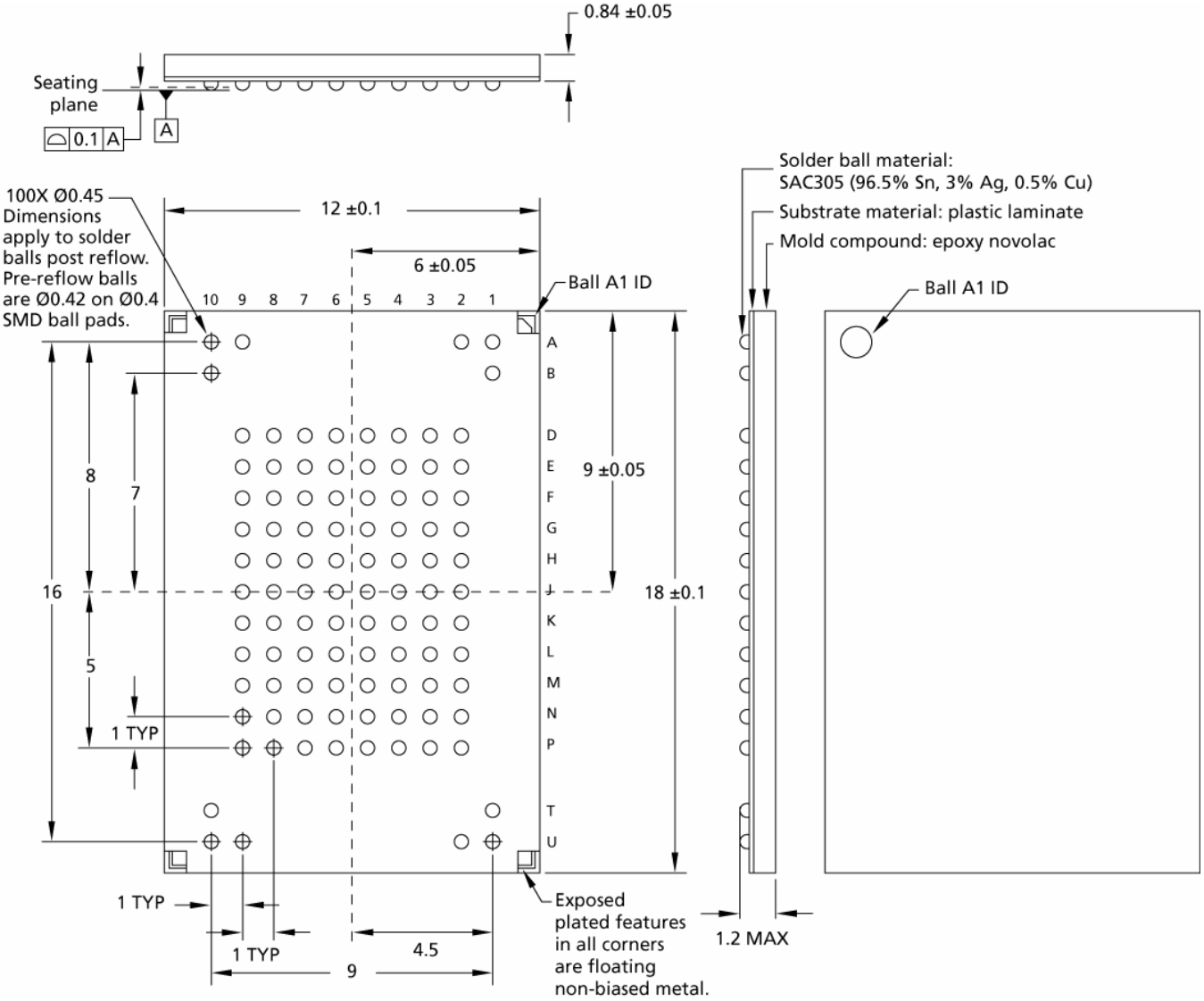
Package Dimensions

Figure 101: 100-Ball VBGA (Package Code H1), 12×18



1. All dimensions in mm.

Figure 102: 100-Ball TBGA (Package Code H2), 12×18



1. All dimensions in mm.

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Revision History

- Rev 0.95, Advance

  Corrected status register bit 1 (FAILC) to remove that it is affected by erase-series operations

  Added DQx to Table 3 on page 16 and Table 4 on page 24.

  Updated the parameter page table.

  Minor corrections.

- Rev 0.92, Advance

  Clarified front page I/O read and I/O write performance

  Corrected error in parameter page bytes 108-109, also modifying bytes 254-255

  Corrected GET FEATURES EFh section to indicate that data output is only updated on the rising edge of DQS.

  Cleaned up many figures throughout

- Rev 0.9, Advance

  Initial draft for NDA customers.